寄附講座：パワーエレクトロニクス寄附研究部門（京三製作所）の 5 年間の活動報告

2024 年 3 月 31 日　寄附講座　河村

1．寄附講座の概要：

寄附研究部門の名称　：　パワーエレクトロニクス寄附研究部門

寄附金額（予定）

総額 100,000 千円（20,000 千円×3+2（延長）年間）

寄附の時期及び期間

2019 年 4 月 1 日より 5 年間（2024 年 3 月 31 日まで）

（諸般の事情により、2021 年度は 13,000 千円に減額）

実際の金額は、93,000 千円（5 年間）

担当教員名及び職名

河村　篤男　寄附講座等教員（教授相当：2019 年 4 月 1 日～2024 年 3 月 31 日）

小原　秀嶺　寄附講座等教員（講師相当：2019 年 4 月 1 日～2022 年 3 月 31 日）

Hadi Setiadi　　寄附講座等教員（講師相当：2022 年 4 月 1 日～5 月 31 日）

Van-Ling Pham　寄附講座等教員(講師相当：2022 年10 月1 日～2023 年1 月31日)

設置目的

横浜国立大学におけるパワーエレクトロニクス関連の研究を一層活発化すると共に，横浜国立大学の教育研究の国際化を更に促進し，その成果を社会に発信することにより，社是に則り，社会貢献するため。

2．5年間の活動報告：

2.1．研究関連：

（1）2019 年 4 月 1 日～2022 年 3 月 31 日：

科学研究費基盤 S（**効率 99.9%級のエネルギー変換が拓く持続的発展可能グリーン社会の実現：**(資料 A：最初の 3 年間の寄附講座活動報告資料の資料 1)）の研究実施期間の後半の 3 年間と寄附講座の前半の 3 年間が重なったので、寄附講座の予算で主として人件費を支払い、研究費は基盤 S の予算を当てた。提案している高効率 HEECS インバータを用いて、最高変換効率 99.827%±0.009%（1300W 出力時）を実測した。詳しい成果や公表論文などは（資料 A の資料 1-2）を参照のこと。

（2）2022 年 4 月 1 日～2024 年 3 月 31 日：

最初の 3 年間で未解決の課題を遂行した結果、(A):さらに高い効率を実測し、効率 99.836% ±0.006%(1300W 出力時)のデータを得た。(B): 太陽光発電機器への応用として、力率制御を検討し、進み力率および、遅れ力率での運転を実証した。詳しい成果や公表論文などは（資料 B:2 年延長分の寄附講座活動報告の資料 1）を参照のこと。

2. 2. 国際化および社会貢献

国内外の招待講演および国外からの見学者受け入れなどを通じて、国際化及び社会貢献を実施した。前半3年間と後半２年間の詳しい資料は、（資料Aの資料2および、資料Bの資料2）を参照のこと。

2.3 研究成果発表の統計データ

上記の活動をまとめて、発表論文（ジャーナル論文、国際会議論文、口頭発表論文）および招待講演の数を表１に示した。

表１　寄附講座の研究活動の統計資料

	ジャーナル論文	国際会議論文	口頭発表論文	招待講演
2019年度	5	3	3	5
2020年度	4	0	7	3
2021年度	4	1	11	3
2022年度	3	0	3	4
2023年度	2	1	4	7
計	18	5	28	22

3. 自己評価

当初の寄附講座の設置趣旨を十分遂行している。

添付資料一覧

資料A：最初の3年間の寄附講座：パワーエレクトロニクス寄附研究部門の活動の報告資料（全35頁）

（構成は以下：）

本文

資料1-1：基盤研究（S）研究進捗評価

資料1-2：基盤研究（S）研究成果報告書

資料2：パワーエレクトロニクス寄附講座の招待講演および海外訪問者

参考資料：寄附講座延長の2年間の研究計画（2022-2023年度）

資料B：延長分２年間の寄附講座：パワーエレクトロニクス寄附研究部門の2年延長分の活動報告（全37頁）

（構成は以下：）

本文

資料1： 発表論文

資料2：パワーエレクトロニクス寄附講座の招待講演および海外訪問者など

添付資料：主要な論文；3編

（以上）

資料 A:

最初の 3 年間の
寄附講座：パワーエレクトロニクス寄附研究部門（京三製作所）の活動の報告資料(35 頁)
の
カバーページ

寄附講座：パワーエレクトロニクス寄附研究部門（京三製作所）の活動の報告資料

2022 年 6 月 13 日　寄附講座　河村

1．寄附講座の概要：

寄附研究部門の名称　：　パワーエレクトロニクス寄附研究部門

寄附金額(施設設備等を併せて寄付する場合はその概要)

総額 60,000 千円（20,000 千円×3 年間）

寄附の時期及び期間

2019 年 4 月 1 日より 3 年間（2022 年 3 月 31 日まで）

（諸般の事情により、2021 年度は 13,000 千円に減額）

実際の金額は、53,000 千円（3 年間）

担当教員名及び職名

河村　篤男　寄附講座等教員（教授相当）

小原　秀嶺　寄附講座等教員（講師相当）

設置目的

横浜国立大学におけるパワーエレクトロニクス関連の研究を一層活発化すると共に，横浜国立大学の教育研究の国際化を更に促進し，その成果を社会に発信することにより，社是に則り，社会貢献するため。

2．3年間の活動報告：

2.1. 研究関連：科学研究費基盤 S（**効率 99.9%級のエネルギー変換が拓く持続的発展可能グリーン社会の実現**）の実施

中間評価では、A 評価を受けた。（令和 2 年 10 月 8 日資料 1-1）また、最高変換効率 99.83%を実測し、研究プロジェクトは 2022 年 3 月末で終了した。（資料 1-2）なお、最終評価は、2022 年度後半の予定

2.2. 国際化および社会貢献（資料2）

国内外の招待講演および国外からの見学者受け入れなどを通じて、国際化及び社会貢献を実施した。

３．自己評価

当初の寄附講座の設置趣旨を十分遂行している。

参考資料：2022-2023年度の方針

2019-2021年度の寄附講座の枠組みを2年間延長する。研究としては、2022年3月時点（科研基盤S終了時）での未解決課題（変換効率99.90％の実証）を遂行する。（詳細は参考資料）

添付資料一覧

資料1-1：基盤研究（S）研究進捗評価

資料1-2：基盤研究（S）研究成果報告書

資料2：パワーエレクトロニクス寄附講座の招待講演および海外訪問者

参考資料：寄附講座延長の2年間の研究計画（2022-2023年度）

科学研究費助成事業（基盤研究（Ｓ））研究進捗評価

課題番号	17H06147	研究期間	平成２９(2017)年度 ～令和３(2021)年度
研究課題名	効率99.9%級のエネルギー変換が拓く持続的発展可能グリーン社会の実現	研究代表者 （所属・職） （令和２年３月現在）	河村　篤男 （横浜国立大学・大学院工学研究院・名誉教授）

【令和２(2020)年度　研究進捗評価結果】

評価		評価基準
	A+	当初目標を超える研究の進展があり、期待以上の成果が見込まれる
○	A	当初目標に向けて順調に研究が進展しており、期待どおりの成果が見込まれる
	A－	当初目標に向けて概ね順調に研究が進展しており、一定の成果が見込まれるが、一部に遅れ等が認められるため、今後努力が必要である
	B	当初目標に対して研究が遅れており、今後一層の努力が必要である
	C	当初目標より研究が遅れ、研究成果が見込まれないため、研究経費の減額又は研究の中止が適当である

（意見等）

本研究では、5kW 級の電力変換器（インバータ）において、変換効率９９．９％に近い効率が実現可能であることを確認し、それを用いて電力配電ネットワークに分散電源を自由に配置できることを実証することを目標としている。

これまでに、規約効率を精密に再評価し９種類の損失を定義してそれぞれ最適化することで、単相高効率チョッパ(HEECS)の効率を９９．７１％まで高めている。実験結果はこの定義と最適化が高効率化に直結していることを示しており、最終年度には当初目標に達すると予想され、研究は順調であると判断できる。新たに考案した損失分解法はこれまでに比べて明快であり、学術のみならずさまざまな電力変換における標準としても使用できるレベルにあり、産業においても貢献度が高い。これらの研究成果については、学術発信も多くなされている。

様　式　Ｃ－１９、Ｆ－１９－１、Ｚ－１９　（共通）

科学研究費助成事業　　研究成果報告書

令和　４ 年　 ５ 月　 ９ 日現在

機関番号：１２７０１
研究種目：基盤研究(S)
研究期間：2017～2021
課題番号：１７Ｈ０６１４７

研究課題名（和文）効率99.9%級のエネルギー変換が拓く持続的発展可能グリーン社会の実現

研究課題名（英文）Realization of Sustainable Green Society Through 99.9% Class Efficiency Electric Power Conversion

研究代表者
河村　篤男（KAWAMURA, ATSUO）

横浜国立大学・大学院工学研究院・名誉教授

研究者番号：８０１８６１３９

交付決定額（研究期間全体）：（直接経費）　 138,000,000円

研究成果の概要（和文）：5kW級のHEECSインバータにおいて、①損失の内訳を実測する損失分解法（測定精度0.04%）を提案して、損失の内訳を明らかにした。②測定精度をさらに1桁高めた仮想トランス非同期同一機器損失測定法（VTALSM法）を提案した。③この測定法を用いて、パラメータの最適を行った結果、SiCパワーデバイスでは電力変換効率99.827%±0.009%を、GaNパワーデバイスでは、電力変換効率99.817%±0.004%を達成した。④このインバータ回路の応用として、力率を自由に変えられ、かつ高速応答運転ができる系統連系動作を実現し、さらに三相HEECインバータによる高効率三相モータ駆動を実証した。

研究成果の学術的意義や社会的意義
我が国のエネルギー事情としては、省エネルギー化および再生可能エネルギーの利用が、持続可能な産業の発展に必須である。再生可能エネルギーの安定利用を実現するための基礎となる技術は、電気エネルギーの変換技術である。本プロジェクトでの成果である99.9%級の電力変換器は電力網のどこへでも配置することができるので、電気エネルギーの利用形態が画期的に変化する。その理由は、電気エネルギーの移動に伴う損失が無視できることにより、周波数、振幅、位相、接地といった電力の移動の制約から解放され、さらに損失が小さいので発熱の制約からも解放され、電力変換機器自体を小型化できるためである。

研究成果の概要（英文）：We proposed a loss decomposition method (measurement accuracy: 0.04%) and clarified the breakdown of losses. Furthermore, a virtual transformer based asynchronous loss measurement method (VTALSM method) was proposed to improve the measurement accuracy by one order of magnitude. Using VTASLM method and the proposed HEECS inverter, we optimized various parameters and controls and achieved power conversion efficiencies and accuracy of 99.827% ± 0.009% for SiC power devices and 99.817% ± 0.004% for GaN power devices. As an application example, we proposed and demonstrated a fast response of powering and regenerating control of grid connected operation. In addition, it was demonstrated that the power factor was freely changed. We also demonstrated the basis of a phase shifter in the power transmission line using the proposed HEECS inverters. As another application a highly efficient three-phase motor drive was demonstrated using three phase HEECS inverter.

研究分野：電気電子工学

キーワード：電力変換　高効率インバータ　電力工学　電気機器

１．研究開始当初の背景

東日本大震災後、我が国のエネルギー事情は苦しい状況に置かれ、省エネルギー化を推し進め、再生可能エネルギーの利用を促進することにより、持続可能な産業の発展を促す状況が続いている。再生可能エネルギーの安定利用を実現するための一番基礎となる技術は、電気エネルギーの変換技術である。例えば、直流を異なる電圧に変換するチョッパや直流電力を交流電力へ変換する数 kW 級のインバータを、99.9%近い電力変換効率で運転できれば、この変換器を電力網のどこへでも配置できるので、電気エネルギーの利用形態が画期的に変化する。現状は効率が高いと言えども従来型の機器（変圧器、変圧器タップチェンジ、メカニカルな開閉器など）と比べて、エネルギーの変換効率が低い（現状の一般的な数 kW 級のインバータの効率は 95～96%程度、電力密度は 1～2kW/ℓ 程度である）ことが障害となっている。本研究では、電力エネルギー網のあり方を画期的に変革するための基礎技術（効率 99.9%級電力変換器）の実証と高効率かつ自由に電気エネルギーが移動可能な電力配電系実現を明示することを目的とする。その結果、持続発展可能なグリーン社会が実現される。

２．研究の目的

本研究では、電力エネルギー網のあり方を画期的に変革するための基礎技術（効率 99.9%級電力変換器）の実証と高効率かつ自由に電気エネルギーが移動可能な電力配電系実現を明示することを目的とする。

具体的には、5kW 級の電力変換器（インバータ）において、変換効率 99.9%に近い効率が実現可能であることを実証し、それを用いて電力配電ネットワークに分散電源を自由に配置できることを実証する。第一段階では、効率 99.9%級の単相インバータ、第二段階では、効率 99.9%級の三相インバータの実現を実証する。第三段階では、このインバータで太陽光発電システムの高速潮流制御が可能なことを示す。第四段階では、このインバータを用いて低圧系の複数の分散電源（電気自動車バッテリ（V2G）、太陽光発電システム）の高効率連携運転を実証し、超高効率インバータで連系したマイクログリッドが、省エネかつ安定に電圧制御が可能なことを実証する。再生可能エネルギーなど時間変動の大きいエネルギーの有効利用のための各種問題が解決される。

３．研究の方法

本研究では、電力配電網において自由なエネルギー移動を可能とするための効率 99.9%級の電力変換器の実現とその運用に関して、研究目的を5つの具体的な研究計画に分類し、逐次推進する。また、電気機器学、制御工学から電力工学の分野に精通した研究分担者と有機的に連携しながら、研究を効率的かつ効果的に推進する。平成 29 年度では、変換効率 99.9%級のインバータを具体化し、試作機 1 号機を製作する。平成 30 年度は三相インバータで効率 99.9%を実証する。平成 31 年度は高効率インバータで系統連系動作を確認する。令和 2 年度は、低圧系マイクログリッドにおいて、変動の激しい複数の分散電源のパワーと電圧の制御が高速に実現できることを実証する。令和 3 年度は、高効率電力変換により電力エネルギー網の構成を変革できることを示す。

具体的には、5年間の研究期間において、次のAからEまでの5つの研究計画に分類し、並列して段階的に研究を遂行することで、研究目的を確実に達成する。

研究計画A：変換効率 99.9%級の 5kW 単相インバータの実現
研究計画B：変換効率 99.9%級の 8kW 三相インバータの実現
研究計画C：この変換器に適した系統連系動作の高速応答技術の確立
研究計画D：低圧系マイクログリッドでの実証実験
研究計画E：電気エネルギー配電網の改革の指針

４．研究成果

4.1 HEECS インバータの基本回路と基本動作

提案する高効率インバータの基本回路と代表的な動作波形は図 1 に示した通りで、これは HEECS インバータと呼ばれている。3 レベルチョッパと折り返し回路の組み合わせによって、スイッチング損失と導通損失のトレードオフをできるだけ切り分けて設計でき、さらにフィルタは DC フィルタで済むので、出力波形は歪の少ない正弦波にできる特徴がある。試験装置の外観は図 2 に示した。

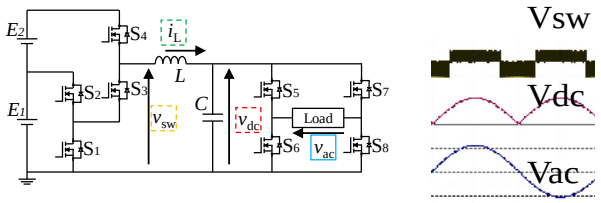


図 1 HEECS インバータ回路（左）と代表的な実測波形（右）

図 2 測定器を含む実験装置の外観

4.2　測定精度向上と実測した最大電力変換効率

4.2.1 損失分解法：

精度よく損失を測定する手法として、個別に全損失を測定する損失分解法を提案した。すべての要素の損失を測定するために、数多くの測定が必要になる。具体的には、1 動作点の効率を求めるために、スイッチングデバイスのスイッチング損および導通損など 9 種類（総測定数 500 点程度）のデータを測定し、各種演算して計算した。その結果、精度は±0.04%(従来法では、±0.36%)となることがわかり、効率としては 2.2kW 出力時に 99.71%となった。

4.2.2 仮想トランス非同期同一機器損失測定法（VTALSM 法）：

効率が 99. 9%に近付くと、さらに測定精度の良い損失測定法が求められる。図 3 に示すように、測定機器は 1 組だけ使用して、インバータの力行と回生の動作点で電力を測定することにより、インバータの力行と回生の損失を高精度で測定する手法を提案した。さらに測定精度の式を導出し、測定精度およびその誤差成分も求めた。この測定法の特徴は、①電力測定器の同一電力（例えば、力行運転時）の差電力測定が高精度に行えることを利用する点、②測定系は被試験機器と 1 組の測定器で構成できるので、測定は力行と回生を非同期で行えること、③測定精度の理論式が導出できたので、測定データごとに測定精度が求まること、④力行と回生の平均効率（平均損失）が求まること、などである。図 4（上）は測定効率の例であり、図 4（下）はその測定精度である。

4.2.3　パラメータ最適化による最大効率の追求：

この測定法を使って、各種パラメータの最適化を行い、損失の最小化を検討した。自由度を基本仕様、前提条件、準仕様パラメータ、自由パラメータに分類して最適化を行った。

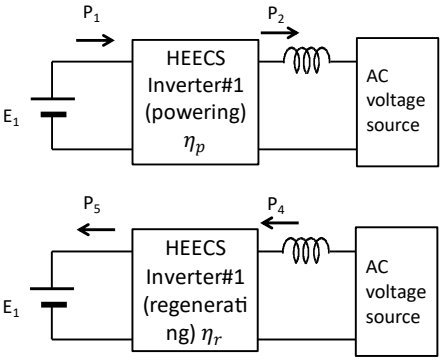
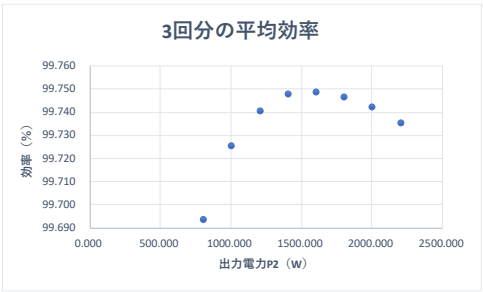


図 3 VTASLM 測定系(上:力行、下:回生)



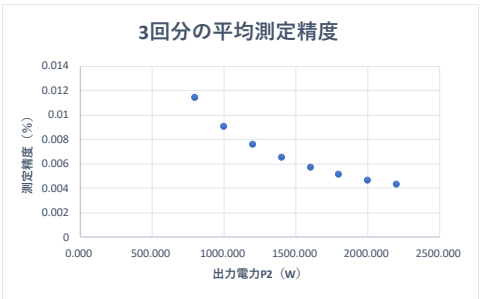


図 4　VTASLM 法による変換効率（上）とその測定精度（下）

図 5　SiC HEECS インバータの写真

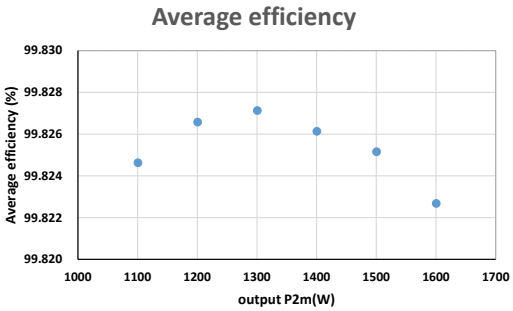


図 6　SiC HEECS インバータの最高効率測定データ（最大効率 **99.827%±0.009%**）

4.2.3(1) SiC パワーデバイスでの最大効率：工夫したパラメータは、パワーデバイスの選定、LC の選定、E_1E_2 電圧の配分比、ゲートドライバ回路、力行回生の電力制御、電流センサレス制御、PCB 基板の設計などである。その回路基板は図 5 に示した。最大電力変換効率は図 6 に示したように、出力 1300W の時に **99.827%±0.009%** を実測した。（測定精度の図はスペースの制約で省略）

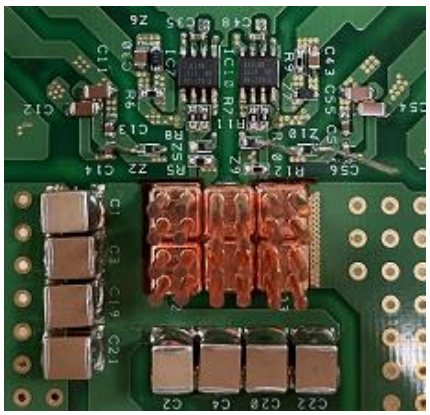


図 7　GaN HEECS インバータの写真

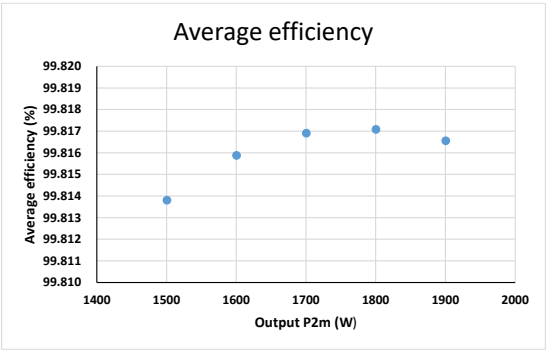


図 8　GaN HEECS インバータの最高効率測定データ（最大効率 **99.817%±0.004%**）

4.2.3(2) GaN パワーデバイスでの最大効率：工夫したパラメータは、前節の項目以外に、①GaN ベアチップの直接 PCB 配線、②ハイサイドとローサイドのデバイスのスイッチの無駄時間を負荷電流に依存した可変デッドタイム制御を実装した。特に、浮遊インダクタンスを低減するために、図 7 に示したように、リフローという手法によりチップを実装した基盤を試作した。測定した効率は、図 8 に示したように、出力 1800W の時に **99.817%±0.004%** となった。（測定精度の図はスペースの制約で省略）

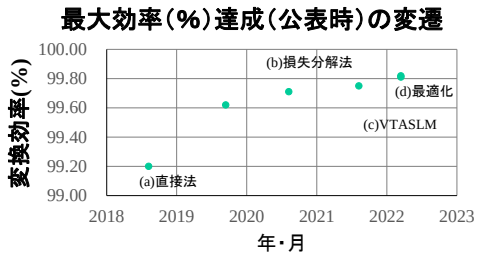


図 9　最大効率測定値の変遷図

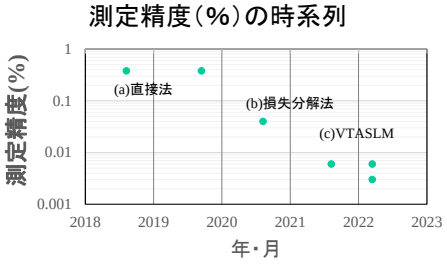


図 10　効率の測定精度の変遷図

4. 2. 4.　最大効率および測定精度の変遷：本報告者のグループが達成したデータを図 9 および図 10 に示した。目標値である効率 99.9%へ向かって向上しているが、本プロジェクト終了時では 99.827%が最大となった。2022 年 3 月の時点での論文サーベイによると、最大効率の文献調査結果は、図 11 となり、最大効率も測定精度も世界最高値と思われる。

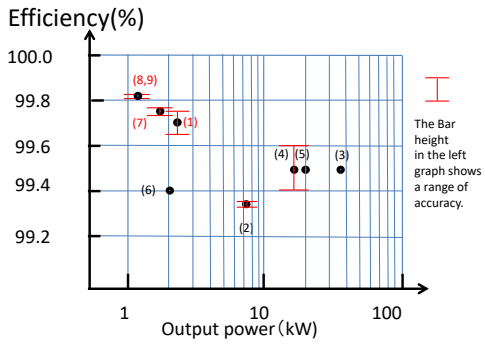


図 11　インバータ最大効率の文献比較

（番号は文献を意味する。1,7,8,9 が本報告者のグループ）

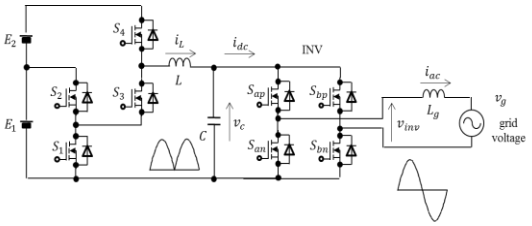


図 12 HEECS インバータの系統連系の結線図

4.3 2 種類の応用検討

4.3.1.系統連系インバータとしての力率制御：

HEECS インバータを系統連系に用いると図 12 のような結線図となる。デッドビート制御に基づく電流制御により、電力の力行から回生への変化は数 ms で実現される。この代表的な実験過渡波形を図 13 に示した。この図では、5ms で力行から回生へ急変している。この制御には、高速な過渡現象の制御と電力の制御が実装されている。また、力率が 1 以外でも動作する制御を考案して実装した。系統から見て遅れ力率動作（インバータから見て進み力率運転）は分散電源による受電端子電圧抑制の観点から重要な要求性能となる。提案制御による端子電圧抑制機能も確認した。さらに、3 相インバータを提案し、系統連系動作を行い、回生や力行動作が実現できることも実証したので、位相器としても動作できる。

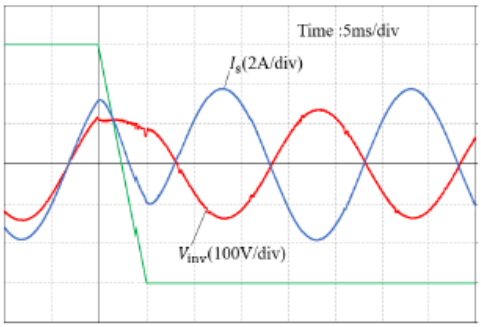


図 13 力行から回生への高速制御波形（青：連系電流、赤：インバータ電圧、緑：電力指令値）

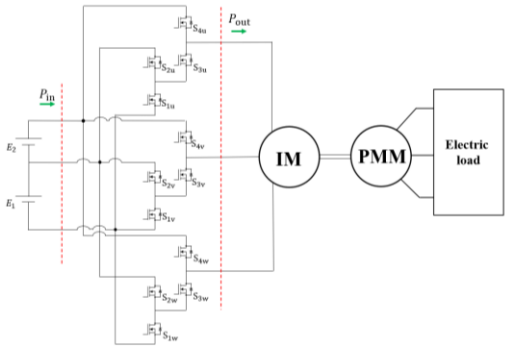


図　14　HEECS 三相インバータによるモータ駆動系の結線図

4.3.2.三相 HEECS インバータによるモータ駆動：

図 14 に示した新しい回路（三相インバータ）を提案した。特徴は、図 1 に示した LC フィルタが必要ないことである。誘導機を駆動する装置を試作して、このインバータの高効率駆動の測定データ（99.52%）を取得した。

4.4.まとめ

①損失分解法（測定精度 0.04%）を提案して、損失の内訳を明らかにした。さらに、測定精度を 1 桁高めた仮想トランス非同期同一機器損失測定法（VTALSM 法）を提案した。

②この測定法を用いて、各種パラメータや制御の最適を行った結果、SiC パワーデバイスでは電力変換効率 **99.827%±0.009%** を、GaN パワーデバイスでは、効率 **99.817%±0.004%** を達成した。

③応用として、系統連系時には高速応答を示す制御を提案し実証した。さらに、力率を自由に制御できる系統連系動作を確認した。さらに、3 相 HEECS インバータを提案し、系統連系動作を確認した。

④三相 HEECS インバータにより三相モータ駆動が高効率で実現できることを実証した。

⑤高効率で自由に電気エネルギーが移動可能な電力配電系実現の基礎（位相器）を実証した。

以上の結果を数行で要約する。電気エネルギーの形態を DC から AC へ変換するインバータにおいて、理学的な見地から損失最小化に挑戦した結果、現状の技術では、効率 99.827%±0.009% が達成でき、2 種類の応用例を実証した。このような技術が実用化されれば、再生可能エネルギーなどの分散電源を多用した電力の配電システムの性能を大きく変えることができ、カーボンニュートラルな社会（持続的発展可能グリーン社会）が実現できる。

５．主な発表論文等

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２．論文標題 Minimization of DC-Link Capacitance and Improved Operational Performance of a 5-Level Hybrid Multilevel DC-Link Inverter	５．発行年 2022年
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Yu Hosoyamada, Itsuo Yuzurihara, Yasutaka Fujimoto, and Atsuo Kawamura

２．発表標題
High-Speed High/Low Pulse Operation by Deadbeat Control Considering Control Delay in Three-Phase Interleaved DC/DC Converter

３．学会等名
IEEE Energy Conversion Congress and Exposition (ECCE2018)（国際学会）

４．発表年
2018年

１．発表者名
伊藤 正悟，永井 栄寿，中﨑 智志，小原 秀嶺，河村 篤男

２．発表標題
インバータの超高効率化に向けた主回路およびフィルタの効率に関する実験的検討

３．学会等名
電気学会全国大会

４．発表年
2018年

１．発表者名
中﨑 智志，永井 栄寿，伊藤 正悟，小原 秀嶺，河村 篤男

２．発表標題
DC-DCコンバータにおける全波整流出力波形生成のためのデッドビート電圧制御の実験検討

３．学会等名
電気学会全国大会

４．発表年
2018年

１．発表者名
海原 拓朗，田村 文太郎，石橋 隆之，河村 篤男

２．発表標題
2電源HEECSパワートレインにおけるSoCアンバランス問題解決に向けた制御手法の提案

３．学会等名
電気学会全国大会

４．発表年
2018年

１．発表者名
石橋 隆之，田村 文太郎，海原 拓朗，弦田 幸憲，河村 篤男

２．発表標題
2電源HEECSチョッパを用いたEVテストベンチでのモード走行効率測定

３．学会等名
電気学会全国大会

４．発表年
2018年

１．発表者名
Atsuo Kawamura

２．発表標題
Activities of IEEJ and IEEJ/IAS and research on High efficiency energy conversion on mobile vehicles

３．学会等名
University Workshop at Chonnam National University and KERI（招待講演）

４．発表年
2018年

１．発表者名
Ayataro Tamura, Koji Kobayashi, Yukinori Tsuruta, Kazuaki Kojima, Hidemine Obara, and Atsuo Kawamura

２．発表標題
Range Extension of Electric Vehicles by Two Battery HEECS Chopper based Power Train

３．学会等名
IEEE ECCE2017（国際学会）

４．発表年
2017年

１．発表者名
Masaya Katayama, Tatsuki Ohno, Hidemine Obara, and Atsuo Kawamura:

２．発表標題
Study on Application of Multi-Level Converter to Realize Fast Current Control in DC Micro-Grid with Extremely Low Impedance Interconnections

３．学会等名
IEEE International Conference on Power Electronics and Drive Systems(PEDS)（国際学会）

４．発表年
2017年

１．発表者名
Tatsuki Ohno, Masaya Katayama, Hidemine Obara, and Atsuo Kawamura

２．発表標題
Flying-Capacitor Linear Amplifier to Realize Both High-Efficiency and Low Distortion for Power Conversion Applications Requiring High-Quality Waveforms

３．学会等名
IEEE International Conference on Power Electronics and Drive Systems(PEDS)（国際学会）

４．発表年
2017年

１．発表者名
Sakahisa Nagai, Robert Oboe, Tomoyuki Shimono, and Atsuo Kawamura

２．発表標題
Fast Force Control Using Acceleration-aided Kalman Filter and Reaction Force Observer for Probing Systems

３．学会等名
IEEE IECON2017（国際学会）

４．発表年
2017年

１．発表者名
片山 正也，大野 達樹，小原 秀嶺，河村 篤男

２．発表標題
マルチレベルコンバータによる直流マイクログリッドの擾乱抑制効果に関する基礎検討

３．学会等名
平成29年電気学会産業応用部門大会

４．発表年
2017年

１．発表者名
大野 達樹，片山 正也，小原 秀嶺，河村 篤男

２．発表標題
フライングキャパシタ形線形増幅回路の実験検証

３．学会等名
平成29年電気学会産業応用部門大会

４．発表年
2017年

１．発表者名
島津 晃大，下野 誠通，河村 篤男

２．発表標題
リニアモータ用磁気浮上形軸受の基礎研究

３．学会等名
平成29年電気学会産業応用部門大会

４．発表年
2017年

１．発表者名
Atsuo Kawamura

２．発表標題
High Efficiency energy Conversion for mobile vehicles

３．学会等名
IEEE Workshop on Emerging technology of transportation electrification（招待講演）（国際学会）

４．発表年
2017年

１．発表者名
Atsuo Kawamura

２．発表標題
High Efficient Energy Conversion for Mobile Vehicles

３．学会等名
Korean Institute of Power Electronics Annual Meeting（招待講演）（国際学会）

４．発表年
2017年

〔図書〕　計0件

〔出願〕　計1件

産業財産権の名称	発明者	権利者
多段直流チョッパ回路、および電力変換装置	河村篤男、弦田幸憲、小原秀嶺	横浜国立大学
産業財産権の種類、番号	出願年	国内・外国の別
特許、2017-126044	2017年	国内

〔取得〕　計0件

〔その他〕

科研費基盤S：効率99.9%級のエネルギー変換が拓く持続可能グリーン社会の実現
http://www.kawalab.dnj.ynu.ac.jp/j_page/kaken.html

６．研究組織

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考
研究分担者	辻　隆男 (Tsuji Takao) (00432873)	横浜国立大学・大学院工学研究院・准教授 (12701)	
研究分担者	小原　秀嶺 (Obara Hidemine) (50772787)	横浜国立大学・大学院工学研究院・准教授 (12701)	

6．研究組織（つづき）

	氏名 （ローマ字氏名） （研究者番号）	所属研究機関・部局・職 （機関番号）	備考
研究分担者	藤本　康孝 (fujimoto Yasutaka) (60313475)	横浜国立大学・大学院工学研究院・教授 (12701)	
研究分担者	下野　誠通 (Shimono Tomoyuki) (90513292)	横浜国立大学・大学院工学研究院・准教授 (12701)	

7．科研費を使用して開催した国際研究集会

〔国際研究集会〕　計1件

国際研究集会	開催年
Kakenhi final year workshop（科研費最終年度成果国際報告会）	2022年～2022年

8．本研究に関連して実施した国際共同研究の実施状況

共同研究相手国	相手方研究機関			
中国	清華大学			
ノルウェー	SINTEFエネルギー研究所			

寄附講座：パワーエレクトロニクス寄附講座の招待講演および海外訪問者など

2022 年 3 月 31 日現在　寄附講座　河村

1．河村の招待講演など

(1) 河村篤男，「電力変換効率 99.9%への挑戦」、第 49 回 YJC 実装技術セミナー，招待講演、2019 年 6 月 11 日、横浜

(2)河村篤男，「電力変換効率 99.9%への挑戦とその研究の変遷」、永守賞授賞式で招待講演、2019 年 9 月 8 日，京都

(3) 河村篤男，「直列チョッパ方式による自動車の走行距離延伸と変換効率 99.9%の電力変換機器実現への挑戦のインパクト」、第 9 回スマートビークル研究センターシンポジウム（豊田工大）で招待講演，2019 年 10 月 24 日、名古屋

(4) Atsuo Kawamura, ”Challenge to 99.9 % efficiency electric power conversion and the applications”、 IEEE ICRERA2019(International Conference on Renewable Energy Research and Applications), Keynote Speaker at Plenary session, November 4, 2019 (Romania)

(5) 河村篤男，「電気自動車の研究を通しての人材育成の事例紹介と自分で考える基礎俯瞰教育の重要性」、2020 パワエレフォーラム，日本パワーエレクトロニクス協会、2020 年 10 月 30 日（オンライン）、基調講演

(6) Atsuo Kawamura, “Challenge to 99.9 % electric power conversion efficiency for inverter in a few kW power range”, IEEE ECCE-Asia (Energy Conversion and Expo), Plenary Invited Speaker, November 30, 2020 (China) (on-line)

(7) Atsuo Kawamura, “Trend of Very High Efficient DC-DC and DC-AC Power Conversion”, IEEE Asian Energy and Electrical Engineering Symposium(AEEES2021), Plenary Invited Speaker, March 26-28, 2021, Chengdu, China (on-line)

(8) 河村篤男、“電力変換効率 99.9%”のインバータ”、日本学術会議-電気電子工学委員会制御・パワー工学分科会、2021 年 9 月 17 日

(9) Atsuo Kawamura, ”Challenge to 99.9 % efficiency electric power conversion and the applications”、 IEEE ICPES2021(International Conference on Power and Energy Systems), Keynote Speech, December 18-20, 2021 (Shanghai, China)

(10) 河村篤男、“パワーエレクトロニクス”、KISTEC　電子技術科「半導体コース」 IoT／5G に向けた半導体の基礎と応用、2022 年 2 月 2 日

２．小原の招待講演など

(1)小原秀嶺,「ノイズを発生しないパワーエレクトロニクス技術」, キョウデン 5G 時代を支えるための技術紹介セミナー（第一回），東京，2019-11

(2)小原秀嶺,「ノイズを発生しないパワーエレクトロニクス技術」, キョウデン 5G 時代を支えるための技術紹介セミナー（第三回），大阪，2020-2

３．国外からの見学者（写真参照）

(1) Prof. C. Worek from AGH University of Science and Technology, Poland, 2019-4-12

(2) 13 students from Tsinghua University(清華大), 中国, 2020 年 1 月 16 日

写真１：Worek教授

写真2：　清華大学からの見学

４．その他の社会貢献

横浜パワーエレクトロニクスカレッジ(YPEC)を 2020 年 4 月開講、主催は特定非営利活動法人 YUVEC、2020 年 10 月実施のベーシックコース（実験を中心にしたカリキュラム、3 日間）を河村・小原が監修。

写真３：YPEC 講義風景

写真４：YPEC 実験風景

2021 年度は、コロナ禍のため中止。2022 年度は再開予定。

(以上)

寄附講座延長更新後２年間の研究計画　　2022-4-1　河村

１．2022 年 3 月時点(科研基盤 S 終了時)での未解決課題

（１）HEECS インバータの電力変換効率が、99.90%には達しない。

・ただし、測定精度は 0.006%を実現できる手法を提案・実証できた。
(ジャーナル投稿中)。

・現状の 99.83%(ジャーナル投稿予定)は世界記録。

（２）応用としてのモータ制御の HEECS インバータ高効率運転の実証実験が未達。

・モータの考慮する必要がある。

（３）応用としての太陽光発電用 HEECS インバータ力率制御の過渡現象実験が未達。制御則が未完成。

２．2022 年 4 月から 2024 年 3 月までの研究課題など

（１）効率 99.90%を実証する：(これが主テーマ)

手段：回路定数などの最適化。

制御：ロバストな制御。

回路トポロジー：いろいろとアイデアはある。

高精度測定技術：さらに、高精度化を狙う。

科研基盤 B が不採択となって、研究費不足となっている。

目標：99.90%が達成できれば、Engineering Science の成果として Nature に論文を投稿したい(希望)。

（２）応用としての高効率モータ制御の実現

制御の準備ができれば、実験できそうだが、技術的に難しい。

（３）応用としての太陽光発電機器の力率制御の過渡現象実験の実現

制御の準備ができれば、実験する予定。

３．招待講演による SDG's への社会貢献

引き続き、招待講演 (2022 年 6 月現在、2022 年度 4 件、2023 年度 1 件の予定) を通じて、社会貢献する。

(以上)

資料 B:

延長分の 2 年間の
寄附講座：パワーエレクトロニクス寄附研究部門（京三製作所）の 2 年間延長分の活動報告(37 頁)の
カバーページ

寄附講座：パワーエレクトロニクス寄附研究部門（京三製作所）の 2 年延長分の活動報告

2024 年 3 月 29 日　横浜国立大学寄附講座　河村

1．寄附講座の概要：

寄附研究部門の名称　：　パワーエレクトロニクス寄附研究部門

寄附金額

総額 40,000 千円（20,000 千円×2 年間）

寄附の時期及び期間

2022 年 4 月 1 日より 2 年間（2024 年 3 月 31 日まで）

担当教員名及び職名

河村　篤男　　寄附講座等教員（教授相当）

Hadi Setiadi　　寄附講座等教員（講師相当　2022 年 4 月～5 月）

Van-Ling Pham　寄附講座等教員（講師相当　2022 年 10 月～2024 年 1 月）

設置目的

横浜国立大学におけるパワーエレクトロニクス関連の研究を一層活発化すると共に，横浜国立大学の教育研究の国際化を更に促進し，その成果を社会に発信することにより，社是に則り，社会貢献するため。

2．2022年4月から2024年3月までの活動報告のまとめ

2.1．研究関連（資料 1 および添付資料論文参照）

(1) 効率 99.90%の実証

新しいインダクタを製作して、効率を実測した。99.836% (1300W 出力時)のデータを得た。引きつづき損失低減の対策を検討している。

(2) 応用としての太陽光発電機器の力率制御の過渡現象実験の実現

太陽光発電器の応用として、力率制御を検討した。進み力率（インバータから見て）を実現し、遅れ力率（インバータから見て）も実証した。

2.2．国際化および社会貢献（資料2参照）

国内外の学会での招待講演および国外からの見学者受け入れなどを通じて、国際化及び社会貢献を実施した。

3．自己評価（添付資料の研究計画参照）

当初の寄附講座の設置趣旨を十分遂行している。

資料1：2022－2023年度の成果のまとめ- 発表論文

資料2：パワーエレクトロニクス寄附講座の招待講演および海外訪問者など

添付資料：寄附講座延長の2年間の研究計画（2022-2023年度）

および主要な論文；3編

資料１　発表論文など　　寄附講座　河村

（2022 年 4 月 1 日-2024 年 3 月 31 日）

１．論文誌論文

(1) Hidemine Obara, Masaya Katayama, Atsuo Kawamura, Jin Xu, Noboru Shimosato, “A Modular Multilevel DC-DC Converter With Auxiliary Inductor Circuits for Cell Voltage Balancing and Fast Output Response”, IEEE Open Journal of Power Electronics, Vol.3, pp. 391-401, 2022, DOI: 10.1109/OJPEL.2022.3185645

(2) Yasuhiko Miguchi, Hadi Setiadi, Yoshiki Nasu, Hidemine Obara, Atsuo Kawamura, “Control Scheme for Leading Power factor Operation of Single-Phase Grid-Connected Inverter Using an Unfolding Circuit”, IEEE Open Journal of Power Electronics, Vol.3, pp.468-480, 2022, DOI: 10.1109/OJPEL.2022.3190559

(3) Atsuo Kawamura, Yusuhiko Miguchi, Hadi Setiadi, Hidemine Obara, “Survey of 99.9% Class Efficiency DC-AC Power Conversion and Technical Issues”, IEEJ Trans. on Electrical and Electronics Engineering, Vol.18, No.1, pp.6-14, 2023, (invited paper) doi.org/10.1002/tee.23728

(4) Yasuhiko Miguchi, Hidemine Obara, Atsuo Kawamura, “Control Scheme for Lagging Power factor Operation of Single-Phase Grid-Connected Inverter Using an Unfolding Circuit”, IEEE Open Journal of Power Electronics, Vol.5, pp.145-161, 2024, DOI:10.1109/OJPEL.2024. 3351147

(5) Atsuo Kawamura, Yukinori Tsuruta, Hidemine Obara, “3.3 kV High Efficiency DC-DC Power conversion”, IEEJ Journal of Industry Applications, Vol.13, No.xx, pp.xxx-xxx, March 2024 (early access), https://doi.org/10.1541/ieejjia.23013265

２．国際会議

(1)Y. Nasu, Y. Miguchi, H. Obara, A. Kawamura, “High efficiency Three-Phase Inverter for Motor Drive using HEECS Chopper”, International Conference on Advanced Motion Control, AMC2024, Kyoto, Japan, February-March 2024

３．口頭発表論文

(1) 味口、小原、河村、“超高効率単相系統インバータの遅れ力率での運転の改善”、電気学会半導体電力変換研究会 SPC-22-150、2022 年 9 月

(2) 河村、Pham、味口、小原、“HEECS インバータのインダクタのパラメータ変化による効率改善に関する検討”、電気学会全国大会 4-053、2023 年 5 月 11 日

(3) 河村,”高効率電力半寒気が拓く電力化社会の夢：直流配電・再生可能電力貯蔵“、電気学会全国大会シンポジウム“カーボンニュートラルの時代に電気が果たす役割～未来につなぐ夢を語ろう～”の 2 部パネラー、2023 年 3 月 15 日

(4) 味口泰彦、Pham Van Long、小原秀嶺、河村篤男、”超高効率単相系統連系インバータ（HEECS）の遅れ力率での運転:改善その 2 “、電気学会産業応用部門大会 4-053、名古屋、8 月 2023 年

(5) 味口泰彦、Pham Van Long、小原秀嶺、河村篤男、”超高効率単相系統連系インバータ（HEECS）の遅れ力率での運転:改善その 3“、電気学会半導体電力変換研究会、SPC-23-184、新潟（佐渡）、9 月 2023 年

(6) 河村篤男、Pham Van Long、味口泰彦、小原秀嶺、”超高効率 HEECS インバータの損失低減に関する新しい展開、電気学会半導体電力変換研究会、SPC-24-122、新潟（五島）、3 月 9 日 2024 年

(7) 河村篤男、Pham Van Long、味口泰彦、小原秀嶺、”HEECS インバータのインダクタの再製作による効率改善に実験報告“、電気学会全国大会 4-050、徳島、3 月 16 日 2024 年

４．その他

なし。

資料２：パワーエレクトロニクス寄附講座の招待講演および海外訪問者など

2022 年 4 月 1 日から 2024 年 3 月まで　　寄附講座　河村

1．河村の招待講演など

(1) Atsuo Kawamura, ”How to realize 99.9 % efficiency inverter and its applications”、 IEEE CPESE2022(Conference on Power and Energy Systems Engineering) Keynote speech, September 9-11, 2022, Kyoto (on-line)

(2) 河村篤男，“効率 99.9%を目指すパワーコンバータの基礎研究”、e モビリティシンポジウム（東京理科大）、2022 年 9 月 17 日、招待講演

(3) Atsuo Kawamura, “Review of 99.9% Class Efficiency DC-AC Power Conversion and Applications”, VANJ Conference 2022 (Vietnamese Academic Network in Japan), Keynote Speaker, November 26-27, 2022, Tokyo (on-line)

(4) 河村篤男,”電気学会全国大会シンポジウム“カーボンニュートラルの時代に電気が果たす役割～未来につなぐ夢を語ろう～”の２部パネルセッション“C.N.社会に電気が拓く未来の夢を語る”のモデレータ、2023 年 3 月 15 日

(5) Atsuo Kawamura, “How to Accurately Measure the Loss of 99.9% class Efficiency Inverter”, ICMIE (International Conference on Measurement Instrumentation and Electronics), Keynote Speaker, April 14-16, 2023, Hangzhou, China (on-line)

(6) Atsuo Kawamura, ”Future Trend of 99.9% class Efficiency DC-AC Power Conversion and its Applications”, ICPST2023(International Conference on Power Science and Technology), Keynote Speech, May 5-7, 2023, Kunming, China (on-line)

(7) Atsuo Kawamura, ”How can we achieve Inverters with an Efficiency level of 99.9%?”, Academic annual Conference of the Power Electronics Committee of CES (China Electrotechnical Society), Keynote Speech, May 13-15, 2023, Shanghai, China (on-line)

(8) Atsuo Kawamura, ”How far have inverters with an efficiency of 99.9% been able to go ?”, IEEE ICPE2023-ECCE-Asia (International Conference on Power Electronics), Plenary Speech, May 22-25, 2023, Jeju, Korea

(9) Atsuo Kawamura, ”Survey of 99.9% Class Efficiency DC-AC Power Conversion and its Future Applications”, IEEE PSGEC2023 (Power System and Green Energy Conference), Keynote Speech, August 24-26, 2023, Shanghai, China

(10) Atsuo Kawamura, “Recent Survey on 99.9% Class Efficiency DC-AC Power Conversion and the Grid Applications”, 2nd Asian Conference on Frontiers of Power and Energy (ACFPE 2023), Keynote Speech, October 20-22, 2023, Chengdu, China

(11) Atsuo Kawamura, ”99.9% Class Efficiency DC-AC Power Conversion and its Application to Grid Interconnection”, IEEE Energycon2024 (International Energy Conference), Keynote Speech, March 4-7, 2024, Doha, Qatar

２．国内外からの見学者（写真参照）

(1) Dr. Kalyan Gokhale, Technology Manager ABB Milwaukee, USA, 2December 5, 2022
Industrial seminar 10:00-11:00 on December 5
および効率測定に関する意見交換

写真１：Dr. Kalyan Gokhale

(2) ヴァレオジャパンからの見学（2023 年 9 月 6 日）

３．その他の社会貢献

(1) 横浜パワーエレクトロニクスカレッジ(YPEC、主催は特定非営利活動法人 YUVEC)のベーシックコース（3 日間、実験を中心にした講習）を 2022 年 9 月 5 日から 7 日に開講した。さらに、2022 年 12 月 9 日と 2023 年 9 月 15 日に、特別実験Ⅰ（1 日間、パワーデバイスの特性測定の講習）を開催した。

写真 2：ベーシックコース風景

写真 3：特別実験Ⅰ風景

(2) Rohm 社から試供デバイスの提供（2023 年 12 月）

(以上)

添付資料

A-1. 寄附講座更新後の 2 年間の研究計画（削除：資料 A の参考資料と同一のため）

A-2. Atsuo Kawamura, Yusuhiko Miguchi, Hadi Setiadi, Hidemine Obara, “Survey of 99.9% Class Efficiency DC-AC Power Conversion and Technical Issues”, IEEJ Trans. on Electrical and Electronics Engineering, Vol.18, No.1, pp.6-14, 2023, (invited paper) doi.org/10.1002/tee.23728

A-3. Yasuhiko Miguchi, Hidemine Obara, Atsuo Kawamura, “Control Scheme for Lagging Power factor Operation of Single-Phase Grid-Connected Inverter Using an Unfolding Circuit”, IEEE Open Journal of Power Electronics, Vol.5, pp.145-161, 2024, DOI:10.1109/OJPEL.2024. 3351147

A-4 . 河村篤男、Pham Van Long、味口泰彦、小原秀嶺、”超高効率 HEECS インバータの損失低減に関する新しい展開、電気学会半導体電力変換研究会、SPC-24-122、長崎（五島）、3 月 9 日 2024 年

IEEJ TRANSACTIONS ON ELECTRICAL AND ELECTRONIC ENGINEERING
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Invited Review Paper

Survey of 99.9% Class Efficiency DC-AC Power Conversion and Technical Issues

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Yasuhiko Miguchi*, Member
Hadi Setiadi**, Member
Hidemine Obara*, Member

This study provides a survey overview of the literatures with the goal of maximizing the efficiency of DC-AC power conversion from an engineering science perspective. With the advent of wide band gap power semiconductors, the published literature on realizing high efficiency DC-AC converters has increased. Therefore, a literature survey of high-efficiency DC-AC inverters was first conducted. We demonstrated the importance of the measurement accuracy in measuring high efficiency losses, and then presented the literature on new measurement methods, as well as examples of analysis of the breakdown of these losses. Furthermore, we reviewed the literature on high-efficiency inverters. We presented measurement data (99.83%) on an inverter with a high efficiency energy conversion system circuit topology using Silicon Carbide (SiC) and Gallium Nitride (GaN) devices to demonstrate how the procedure was used to achieve loss minimization. We summarized the challenges hindering high efficiency.

Keywords: high efficiency; loss measurement; virtual transformer; measurement accuracy; inverter

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1. Introduction

1.1. Objective of this paper To address the issues of global warming and resource depletion, it is important to improve the efficiency of power conversion. Higher-efficiency power converters are used in several fields, such as electric vehicles and renewable energy generation, for saving a considerable amount of energy. From an engineering perspective, the power density of power converters (Ohashi [1], Google little box [2], Kolar [3]) has been prioritized, and numerous studies have been conducted. This is because, in practice, downsizing and weight reduction of equipment reduce costs and can be applied in various application fields. Few studies have been conducted on power loss reduction from the perspective of engineering science, focusing only on efficiency [4,5]. This is because, no matter how high the efficiency is obtained, if the power conversion system becomes large, it will be a problem in practical use. Therefore, it is important to identify the upper limit of efficiency in the current wide band gap (WBG) devices and clarify the obstacles in the future development of power conversion from the view point of engineering science. In particular, it is important to determine the upper limit of efficiency when improving power density. Therefore, in this study, we conduct a literature survey on how low the loss of DC-AC power conversion can be, and how high the efficiency can be achieved. In addition, we discuss the future trends and technical issues in this challenge.

In the field of DC-DC power conversion, it has been proven that, based on the principle of partial power conversion, the efficiency can be maximally increased in principle if the input–output voltage ratio is fixed to a certain condition [6,7]. However, in DC-AC conversion, this condition is not satisfied because the output voltage varies from zero to positive and negative rated voltages. Accordingly, the input–output voltage ratio varies. Therefore, no general method to minimize losses can be found for DC-AC power conversion [3]. Consequently, the authors proposed to synthesize a full-wave rectified voltage waveform by a multilevel DC-DC converter, which was then folded back to generate a sinusoidal waveform by an unfolding inverter circuit topology inverter called the two-battery high efficiency energy conversion system (HEECS) shown in Fig. 1 [4], and then they published data with efficiencies of over 99.8% [5]. This circuit is unique because it can separate switching and conduction losses and simultaneously minimize them [4,8,9]. As a result, it can achieve a very high efficiency. However, the disadvantage of this circuit topology is that the output current includes a much larger distortion than that of conventional pulse width modulation (PWM) inverters when the load power factor is not unity. However, the authors proposed remedies for the problem [10,11], and by modifying the control algorithm, the HEECS inverter manages to have a low distortion in the output current for various power factors while maintaining high efficiency. Comparison with efficiency improvement using other circuit topologies and motor drive with a three-phase HEECS inverter [12] are discussed in Section 4. To the best of our knowledge, no studies have been conducted

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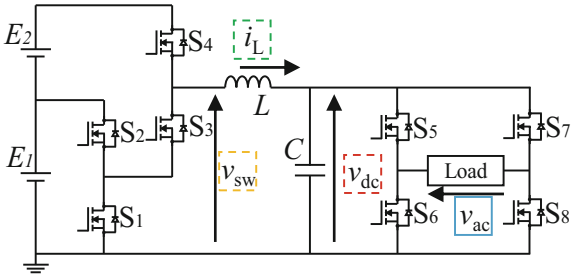

Fig. 1. Two battery HEECS inverter [4,5]

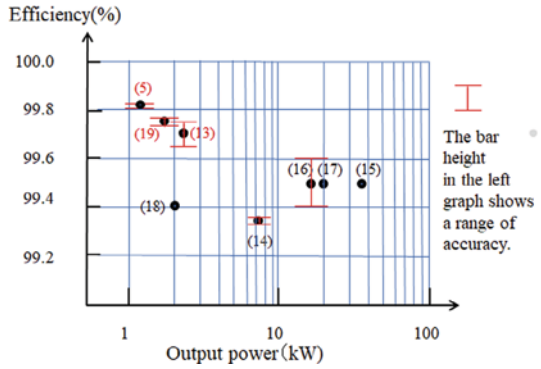

Fig. 2. Survey of high efficiency inverters [5]

that exceed the maximum efficiency achieved by this circuit topology [5].

1.2. Literatures on high efficiency measurement of inverters and importance of measurement accuracy

Several actual measurements of high efficiency of inverters using WBG devices have been reported [5,13–20], and examples of reported output and efficiency, including their measurement accuracy, are shown in Fig. 2. Note that if there is no description of the measurement accuracy in the literature, the accuracy is not indicated. The figure shows that DC-AC conversion efficiencies of 99.5% or higher can be achieved with the latest WBG devices. The height of the bars in the figure indicates the measurement accuracy. When the conversion efficiency is close to 99.9%, then the measurement accuracy is critical. The highly efficient dataset in the upper left corner is a group from the authors' literatures.

It is reported [13,14] that loss measurement by the direct subtraction of the input and output power results in an efficiency accuracy of 0.38%. To measure the total loss accurately, the calorimetric method is adopted [14,21–24]. Historically, induction motor loss was measured by this method [23,24]; however, the insulation of the heat flow was poor, and the leakage of the heat was not well suppressed. Consequently, the measurement accuracy was not high. In Refs. [14,21,22], the whole converter under test was installed in a double-layer-structure of thermal insulated chamber, and the loss was precisely measured by heat flow in this inner chamber. In DC-AC conversion, a high accuracy of 0.003% was reported in Ref. [14]. There are few other approaches for the high accuracy. A loss breakdown approach [13] in all electric measurement accuracy of 0.04% was reported for DC-AC conversion. However, many types of data measurements are required, and the data handling process is complicated.

In Ref. [25], it was reported that by the introduction of a virtual ideal transformer-based Back-to-Back (BTB) measurement, an average efficiency of powering and regenerating operations of inverter can be theoretically measured at the accuracy of 0.002%. This idea was extended to the practical measurement aspect, and a new approach was proposed, known as virtual transformer-based BTB asynchronous loss measurement (VTASLM), using one set of measurement instruments [19], and the accuracy of 0.006% was reported. The measuring procedure is as follows. First, prepare one set of measuring instruments and a power converter under test. Second, calibrate the power measuring instruments. Finally, measure the losses of powering and regenerating operations. This technique was employed in this study. This approach is briefly summarized in Section 2. In addition, based on the measurement from the HEECS inverter loss with respect to the breakdown of losses, we presented and discussed with respect to loss reduction measures.

1.3. Problems in the pursuit of high efficiency—approaches and discussion as for loss reduction

Because the method for measuring losses electrically and with high precision has been established in Ref. [19], we need to establish a method to minimize losses and maximize efficiency. Various approaches can be considered for such a method; however, a fair comparison of the maximum efficiency values cannot be obtained unless common assumptions, such as ratings and circuit parameters are pre-determined. Therefore, in Section 3, we organize these common preconditions, and then define various free parameters for efficiency maximization. Subsequently, we summarize methods for obtaining maximum efficiency [5]. Thereafter, we survey literatures on actual methods to seek the maximum efficiency of HEECS inverters using SiC and GaN power devices. In addition, Section 4 summarizes the discussions regarding the realization of maximum efficiency from the perspective of the relationship between the output capacitance *Coss* of the power device, and the system total resistance, as well as the comparison with other circuit topologies [5].

2. High-Precision Measurement Method and Loss Analysis of DC-AC Converters

2.1. VTASLM method If an ideal transformer can be realized with no voltage amplitude difference or phase shift between the input and output terminals, and zero losses using an electronic load and an AC voltage source, only the losses of the power converter can be measured by the arrangement shown in Fig. 3. To elaborate on this figure, two inverters operating in powering and regenerating are connected via an ideal transformer. At the DC voltage source terminals, the input terminal on the power side and the output terminal on the regenerative side are connected. Therefore, only the powering and regenerating operation losses are supplied from the DC source, and if they can be measured, the total powering and regenerating losses can be obtained [25]. This is the ideal case; however, in reality, an ideal transformer does not exist. In the absence of an ideal transformer, a method to measure the powering and regenerating losses separately is considered, and the detailed measurement procedure and measurement accuracy are analyzed in the literature (19). According to this, as shown in Fig. 4, it is proposed to measure losses during powering and

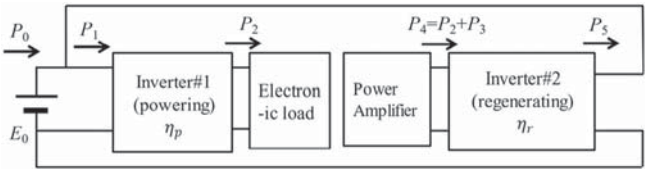

Fig. 3. A BTB loss measurement system based on virtual ideal transformer [19,25]

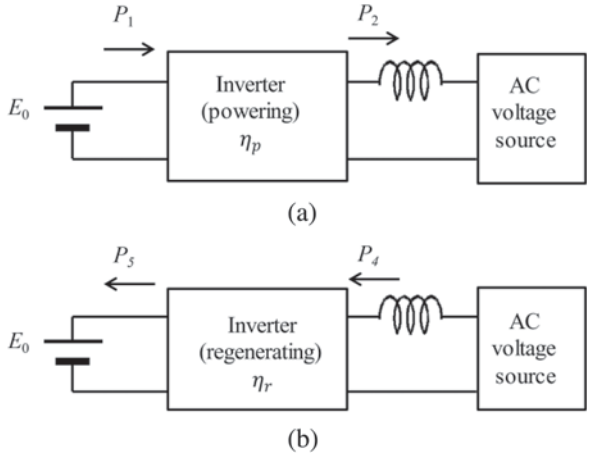

Fig. 4. Basic structure of virtual transformer-based BTB asynchronous loss measurement method using one set of measurement instruments (VTASLM) [19]. (a) Powering power measurement and (b) Regenerating power measurement

regenerating operations asynchronously. However, the proposed method has the following two problems: (1) measurement errors due to the fact that the output of powering power and input of regenerating power are not equal owing to asynchronous operation between Fig. 4(a), (b). (2) measurement error of the measurement instruments because the current flow direction of the current sensor between powering Fig. 4(a) and regenerating Fig. 4(b) is the opposite of each other. A DC offset is observed between the current readings. These problems were analyzed, leading to a proposal of a practical accurate measurement [19] in which a SiC-HEECS inverter was selected as the converter under test. The results showed that the power conversion efficiency is 99.75%, and its measurement accuracy is 0.006% when the output power is 1600 W. Furthermore, the breakdown of that 0.006% measurement accuracy was analyzed in the discussion, and the calibration error owing to the change in current direction is quite large at approximately 60%, followed by a reading error in loss measurement [26,27] at 20%, and a smaller measurement error based on control stability at 15%. All errors were statistically processed, and the measurement accuracy was varied depending on the measurement date.

2.2. Breakdown of losses and loss reduction policy

A measured breakdown of the SiC-HEECS inverter losses has been proposed [13]. All losses were obtained by measurement and theoretical calculations. The losses were divided into (1) switching losses in the DC-DC chopper section, (2) conduction losses in the DC-DC chopper section, (3) losses in the filter inductor, (4) conduction losses in the Printed Circuit Board (PCB), and (5) conduction loss of unfolding inverter. The loss breakdown graph is shown in Fig. 5. Because it is necessary to measure the loss of each device, the number of acquired data is large, and the data processing is also time-consuming. At an output of 2.2 kW, a power conversion efficiency of 99.71%, and a measurement accuracy of 0.04% were obtained.

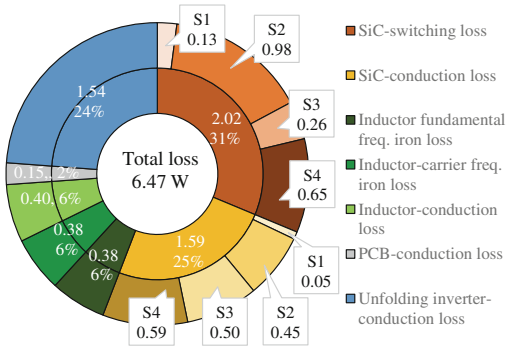

Fig. 5. Loss breakdown ratio of DC-AC conversion (2.2 kW) of SiC-HEECS inverter (symbols S1, S2, S3, and S4 are the same as those in Fig. 1) [13]

From this figure, a policy for loss reduction can be discussed. The power device used in the chopper section is Rohm's SCT3017AL (conduction resistance: 17 mΩ). First, it is necessary to reduce the switching loss in the chopper section; however, it is clear that the selection of the device is important. Devices should be selected from the viewpoints of (1) minimizing switching loss by devising a gate drive system and (2) selecting a device with a minimum conduction loss. Next, unfolding inverters should be selected with a low conduction loss because switching losses can be ignored as switching operations are performed only twice in one cycle. Inductor loss consists of conduction loss, fundamental frequency iron loss, and harmonic ripple iron loss. In addition, the material, switching frequency, and size of L should be properly selected. Finally, the resistance of the printed circuit board (PCB) substrate must be selected to be small. Currently, the thickness is 175 μm, and the loss ratio is small.

3. Optimization of High Efficiency DC-AC Power Conversion and Literature Review

The procedure for the loss optimization is as follows: (1) A basic specification is set so that a fair comparison is made, (2) a circuit topology is selected, (3) quasi-specification parameters are selected for this topology, and (4) free parameters are optimized. Finally, the literature review and new data are introduced.

3.1. Basic specifications and other concepts for fair comparison

A fair comparison of the actual measured values of the maximum efficiency obtained is not possible unless common preconditions, such as ratings (voltage and current) and circuit parameters, are pre-determined. Therefore, common preconditions are organized, and then the preconditions, quasi-specification parameters, and free parameters for efficiency maximization are selected and summarized with respect to the literature (5).

(1) Basic specifications—device voltage margin, switching frequency, and voltage total harmonic distortion (THD)

Table I. Basic specification for inverter under test

Device voltage margin	50% of the output voltage
Switching frequency	16 kHz
THD of output voltage	Approximately 1%

Because the output voltage is related to the rated voltage of the power device, we decided that the voltage margin of the device should be 0.5 times the peak output voltage. There are many ways to make a choice regarding this part; however, if this decision is not made, subsequent developments will be affected. Therefore, we proposed this selection as a benchmark. Specifically, using a device rated at 650 V, the output peak voltage v_{acpeak} of the inverter is expressed by

$$v_{acpeak} = 650 \div 1.5 \approx 433 \quad (1)$$

The sum of the voltages of the two power supplies E_1 and E_2 of the HEECS inverter in Fig. 1 was fixed at this value. Furthermore, the switching frequency was set to 16 kHz, which is considered to be the lowest limit of the non-audible range to humans. Finally, the THD of the output voltage was determined to be approximately 1%. Although IEC61727 [28], a regulation for grid interconnection, specifies, for example, a harmonic current (3rd to 9th order) of 4.0% (10 kW or less); the voltage was specified here. These were considered suggestions for benchmarking in the next section and beyond. The output rating was set at 5 kW. These are summarized in Table I.

(2) Circuit topology: reasons for selection of HEECS circuits

The prerequisite is the circuit topology, and the HEECS inverter circuit shown in Fig. 1 was chosen for this study. This circuit has the following three characteristics, judged from the scientific viewpoint of reducing losses [4,13]. (1) The DC-DC chopper section is a multilevel power conversion, and the principle of partial power conversion inherently allows high power conversion efficiency if the voltage conversion ratio is small [4,6,7]. (2) Because the output voltage operates to output a full-wave rectified waveform, the fundamental flux variation of the inductor is mostly in the first quadrant of the flux density—field intensity (B-H) plane [29], which is considered to have less loss than if the variations were over four quadrants [13]; (3) In the unfolding inverter circuit, switching losses are negligible because the switching operation is once every half cycle, and a device can be chosen to suppress conduction losses. If a circuit topology other than this is chosen, the ideas in the following discussion can be applied, but the procedure will be different. Another circuit topology is discussed in Section 4.2.

(3) Quasi-specification parameters—circuit parameters and free parameters.

The quasi-specification parameters are the material of the switching device of the chopper section (SiC, GaN, etc.), and its voltage and current rating; the material of the LC filter inductor and its inductance; the material of the capacitor and its capacitance; the material of the unfolding inverter device and its voltage and current rating; the output voltage control method; the PCB pattern of the circuit.

Table II. Quasi-specification parameters

Chopper devices	*Ron* = 17mΩ (typ) SCT3017AL (Rohm)
Resistance of unfolding inverter devices	*Ron* = 3.7mΩ CAS325M12HM2 (Wolfspeed)
Inductor *L*	1.25 mH (18 mΩ) (Ferrite) (IPEC)
Capacitor *C*	8 μF (3.5 mΩ) (film) (ARCOTRONICS)
Control	DB(Deadbeat) Powering & regenerating
PCB	175 μm Cu thickness (a few mΩ) (P-ban)

Finally, the free parameters are the voltage ratio of the two power supplies E_1 and E_2, gate driver's ingenious parts according to the circuit topology (gate resistance and dead time between the high and low side of the chopper), and output (load) with the maximum efficiency.

In the following, we focus on the case of SiC power devices, and also introduce a literature for the case of GaN.

3.2. Case study—SiC

3.2.1. Quasi-specification parameters For the SiC switching devices in the chopper section, we selected those with the lowest possible on-state resistance *Ron* (highest possible current rating). Similarly, the unfolding inverter is turned on and off only twice per cycle; thus, we selected a device with the lowest possible on-resistance (highest possible current rating). These are shown in Table II.

Next, ferrite and amorphous are the materials of choice for inductance. Preliminary comparison experiments were conducted to determine the loss owing to differences in materials with similar inductance, and we decided to use a ferrite inductor of 1.25 mH, as shown in Table II. The material used for the capacitor was film, and its capacitance was selected as 8 μF based on preliminary experimental measurements of loss. An improvement in efficiency of approximately 0.001% for 4 μF was achieved compared to that of 8 μF; however, the deadbeat (DB) control described below worked stably in both powering and regenerating modes when using 8 μF; thus, this value was used. There is room for improvement in this selection. The VTASLM method requires both powering and regenerating operations, and the open-loop control of HEECS inverter exhibits a high THD in case of regeneration operation. To guarantee stable operation of HEECS inverter in both powering and regenerating conditions with small THD required in the basic specification in Section 3.1, this DB control was adopted [10,30]. The PCB (175 μm copper thickness) design was fabricated in-house for the pattern, and the hardware was prototyped on a P-ban. The conduction resistance of the circuit is a few mΩ, although the total conduction resistance varies depending on the pattern through which the devices conduct [13].

3.2.2. Free parameters-E_1/E_2 voltage ratio, gate driver, variable dead time control, and sensorless control The remaining degrees of freedom were the voltage ratio of the two power supplies E_1 and E_2, ingenious part of the gate driver according to the circuit topology (gate resistance and dead time distribution between the high side and low side of chopper), and load (resistive) parameters at maximum efficiency.

E_1E_2 ratio The output capacitance *Coss* of the power device determines the magnitude of the current to be charged and discharged for each switching operation, and the charging and discharging power is a function of the voltage between the drain-source (DS) terminals. Switching losses are a function of the switching voltage and current, which are also functions of the voltage between DS terminals. Therefore, the loss owing to these two factors is expected to have a minimum value by changing the ratio of E_1 and E_2 [5,20].

Therefore, we qualitatively considered the following equations. First, assuming EI/6 as an approximate formula for switching loss E_{SW} [31], the approximate E_{SW} and the charge/discharge energy loss E_{coss} owing to the output capacitance *Coss* can be obtained in the following formula.

$$E_{sw} \propto 1/6E_1 \int_0^{\theta_0} I_{ac}d\theta + 1/6E_2 \int_{\theta_0}^{\pi/2} I_{ac}d\theta \tag{2}$$

$$E_{coss} \propto 1/2C_{oss} \int_0^{\theta_0} E_1^2 d\theta + 1/2C_{oss} \int_{\theta_0}^{\pi/2} E_2^2 d\theta \tag{3}$$

where

$$\sin(\theta_0) = E_1/(E_1 + E_2)$$

Plotting the magnitudes of (2) and (3) with E_1 as the variable on the horizontal axis, both curves are convex downward. The minimum point of Eq. (2) is located far to the right of $(E_1+E_2)/2$, while that of (3) are located slightly to the right of $(E_1+E_2)/2$. Figure 6 qualitatively illustrates this trend. Therefore, when E_1 is assumed as a variable and the total loss, including (2) and (3), is measured, it is expected that the total loss shows the minimum point at the certain E_1, which is slightly on the right side of $(E_1+E_2)/2$. Figure 7 depicts the measured loss as a function of E_1 according to the direct method of measurement [13]. In this experiment, the total value of power supplies E_1+E_2 was fixed at 433 V as specified in (1). From Fig. 7, it is observed that the loss is minimized when E_1 is 250 V. Based on the theoretical discussion in this section and experimental results, the loss is considered to be minimized when the free parameter E_1 is 250 V. E_2 is 433−250 = 183 V.

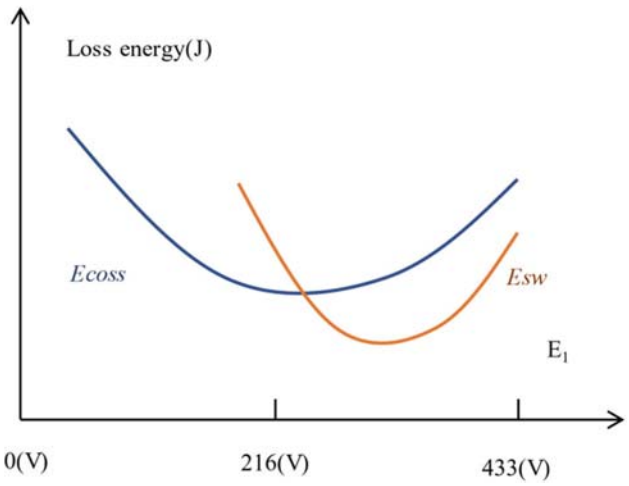

Fig. 6. Qualitative illustration on loss of *Coss* and switching regarding E_1 ($(E_1+E_2)/2 = 216.5$(V))

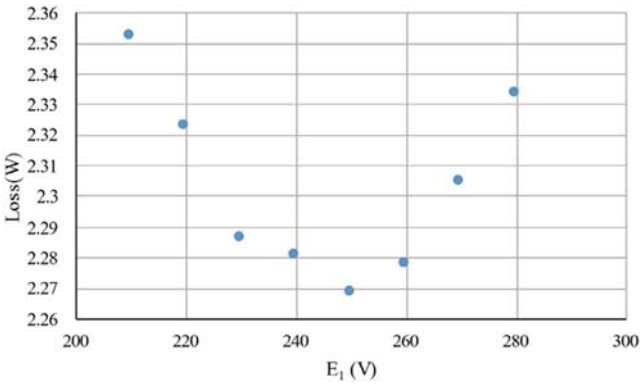

Fig. 7. Relation between loss and E_1 (experiment) [5]

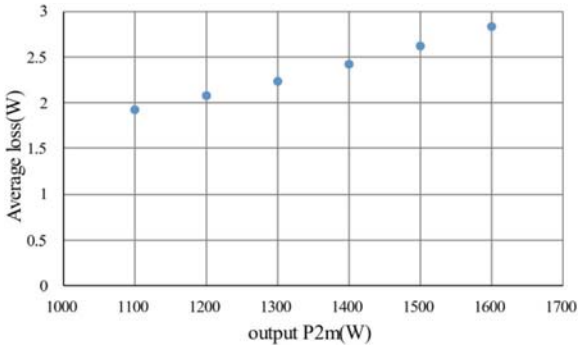

Fig. 8. Measured average loss of SiC-HEECS inverter by VTASLM [19]

Reduced losses owing to improved gate drivers and control laws Measures to reduce losses by adjusting the gate circuit include (1) devising a suitable gate driver [32] and (2) variable adjustment of the dead time between the high side and low side devices [33]. A BM6105FW-LBZ (Rohm) gate driver was used. The use of an active gate drive was investigated [32]; however, the most minimum switching loss was obtained by a trial-and-error approach on gate resistance of driver circuit for the specific PCB. In addition, to match the switching characteristics, the characteristics of the devices were measured using a curve tracer, and devices with uniform characteristics were used for the PCB. In addition, the dead time between the high-side and low-side switches' on and off timing in the chopper circuit was considered as a variable to suppress the losses at the body diode and the unregeneratable loss at *Coss* [33]. Furthermore, instead of using a current sensor to detect the inductor current, a minimum order observer was used for DB control [30]. Consequently, power consumption at the current sensor was reduced.

Measured loss, efficiency, and accuracy results Considering the above improvement measures, the loss, power conversion efficiency, and measurement accuracy are shown in Figs. 8–10 [5]. From these figures, an efficiency of 99.827% ± 0.009% (1300 W output) was observed at SiC-HEECS inverter.

3.3. Case study—GaN Loss measurements were performed using a GaN high power device (GS-065-150-1-D2,

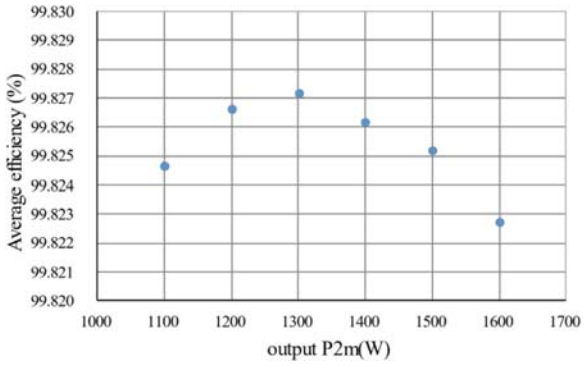

Fig. 9. Measured average efficiency of SiC-HEECS inverter by VTASLM [19]

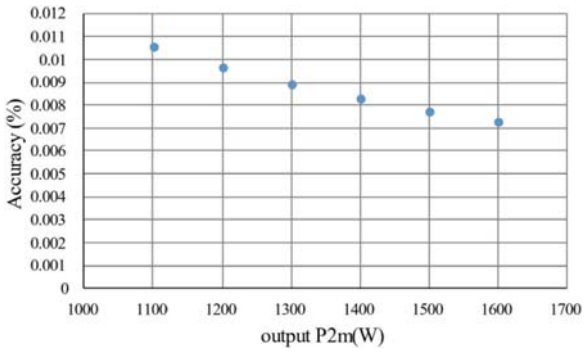

Fig. 10. Accuracy of SiC-HEECS inverter efficiency measurement by VTASLM

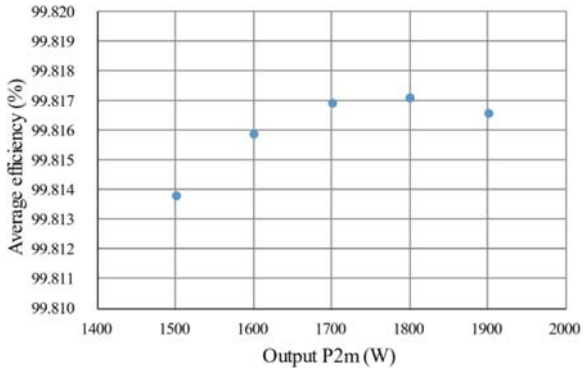

Fig. 11. Measured average efficiency of GaN HEECS inverter by VTASLM [19]

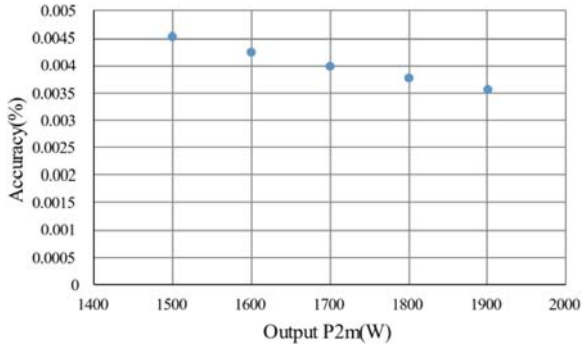

Fig. 12. Accuracy of GaN-HEECS inverter efficiency measurement by VTASLM

GaN System) in the chopper section. The device is rated for 650 V, 150 A, and $Ron = 10$ mΩ. Because it was only available as a bare chip, a direct placement technique was employed by reflow method on a PCB [33]; otherwise, the quasi-specification parameters were set the same as in the SiC case. First, the gate resistance was adjusted by trial and error. Next, the optimum voltage ratio distribution of E_1 and E_2 was determined by the similar measurement as in section 3.2.2.1, and E_1 was selected to be 260 V. Furthermore, owing to the operating mode, the dead time of the upper and lower side devices was adjusted because the voltage drop in the body diode is large owing to WBG devices. Consequently, the loss owing to synchronous rectification operation is significantly reduced, and simultaneously, the loss owing to the unregenerated energy at *Coss* can be reduced; however, the control method could be further improved [33,34] because there is a small phase shift between the inductor current and output voltage due to the LC filter in the HEECS-chopper stage, and this was ignored in this experiment [13]. Furthermore, the current sensorless control was implemented for measurement.

Under these conditions, the efficiency and measurement accuracy were measured by the VTASLM measurement method and are shown in Figs. 11 and 12 [5]. From this figure, a maximum efficiency of 99.817% ± 0.0038% (1800 W output) can be read. Both SiC and GaN had almost the same maximum efficiency; however, GaN showed the maximum efficiency when the output power was higher than that of SiC because the device conduction resistance of GaN is smaller than that of SiC.

4. Discussions

4.1. Discussion on relations between output capacitance *Coss* and minimum loss

4.1.1. Theoretical explanation of loss minimum condition

Assuming that the loss can be approximated by a second-order polynomial as a function of the output P_2 (defined as x), we define the following equation

$$y = a + bx + cx^2 \tag{4}$$

where y is defined as the loss (W) and x is the output power P_2 (W).

The efficiency η can be obtained by dividing the loss by the output power and then subtracting it from 1, as shown below.

$$\begin{aligned}\eta &= 1 - {}^{y}\!/_{x} \\ &= 1 - (b + {}^{a}\!/_{x} + cx)\end{aligned} \tag{5}$$

This equation has a minimum when the third and fourth terms on the right-hand side are equal. That is, when Equation (6) is satisfied,

$$x = \sqrt{{}^{a}\!/_{c}}, \tag{6}$$

the maximum efficiency η_{max} becomes (7),

$$\eta_{\max} = 1 - (b + 2\sqrt{ac}). \tag{7}$$

4.1.2. Case study on SiC devices Applying the results of the previous section to the loss of SiC-HEECS inverter in Fig. 8, the maximum efficiency is obtained by (7), which agrees well with the measured data in Fig. 9. This implies the validity of (4) [5].

Because the output power is measured under the constant output voltage condition, the output power P_2 $(=x)$ can be considered to be proportional to the output current. The coefficient a in (4) is constant regardless of the load, and corresponds to the loss owing to *Coss* discussed in section 3.2.2.1. The coefficient b is for losses that are proportional only to current, such as switching losses. The coefficient c is related to the conduction loss of the entire system, which is proportional to the square of the current. The maximum efficiency increases as the second and third terms on the right side of (7) reduces. Furthermore, the third term $2\sqrt{ac}$ is approximately one order of magnitude larger than the second term b; thus, the maximum efficiency (7) will increase by suppressing this third term. Because the third term is the product of a and c, it can be regarded as proportional to the product of *Coss*, and the total system conduction resistance r_{onall}. Table III shows a survey on this product concerning available devices from various companies. As Company A's device is used in this experiment, it is the smallest. This product is tentatively named as "Efficiency Figure of merit" (EFOM), and is similar to the high-frequency figure-of-merit (BHFFOM [35] and NHFFOM [36]) of the device itself [37]. These indices in Refs. [35–37] were used to evaluate the high-frequency characteristics of the device alone; however, because the discussion here is concerning increase of the maximum efficiency of the system, there is a difference between the efficiency of the device alone (EFOM) and the system, in which the total system conduction resistance r_{onall} should be used as an evaluation of efficiency instead of the device on-state resistance.

4.2. Possible circuit topologies

A circuit similar to the HEECS circuit configuration is the T-type circuit; the HEECS and T-type circuit topologies are shown in Fig. 13 [38]. A step-down DC-DC converter operation was performed with identical filters and load resistors connected as their output circuits, and the losses were measured by the direct method [13]. SiC-MOSFETs with on-resistance of 17 mΩ were used for all switches. For each MOSFET, a Schottky barrier diode was connected in parallel; the supply voltages for E_1 and E_2 were determined by the method proposed in Ref. [39].

Figure 14 shows the efficiency map of the power conversion when the switching frequency is fixed at 20 kHz, and the output voltage is varied [38]. Comparing the HEECS with the T-type circuit topology, the HEECS shows approximately 0.01% higher efficiency over almost the entire measurement range. This may be

Table III. Efficiency figure of merits (EFOM): Product of *Ron* and *Coss*

Voltage & current ratings	650 V–118 A	650 V–64 A	650 V–81 A
Ron (mΩ)	17	22	15
Coss (pF)	148	262	189
EFOM (10–12) (s)	2.5	5.8	4.3
material	SiC	SiC	SiC
company	A	B	C

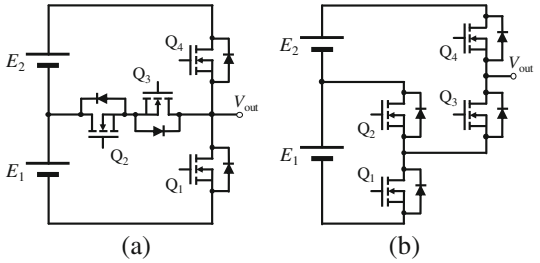

Fig. 13. T-type and HEECS circuit topology [37]. (a) T-type and (b) HEECS

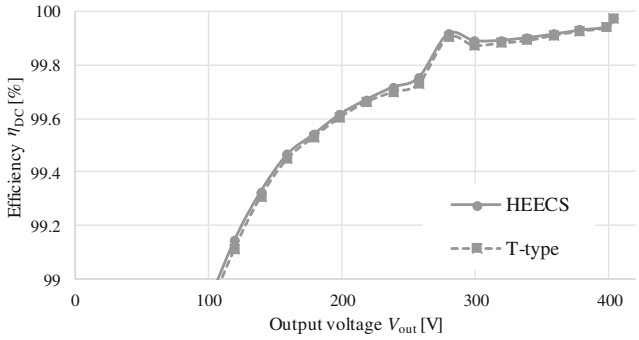

Fig. 14. Comparison of efficiency between T-type and HEECS [37]

owing to the amount of charge in Q_1, which is stored in the device output capacitance *Coss*. In particular, when Q_4 is turned on and off, energy of voltage $(E_1 + E_2)$ is charged and discharged in the *Coss* of Q_1 in the T-type; however, in the HEECS, the voltage is distributed between Q_3 and Q_1, resulting in less charge and discharge energy. Furthermore, when the devices were parallelized to lower the on-resistance, the loss unexpectedly increased further [40]. Therefore, charging and discharging energy of *Coss* increases more than the reduced conduction loss. These phenomena usually result in negligibly small differences in losses; however, in the region of extremely-high efficiency, which is close to 99.9%, this difference becomes significant.

From the view point of reduction of switching loss, previous research suggests the use of modular multilevel cascaded converters (MMCCs) to achieve highly efficient power conversion in inverters [41,42]. Increasing the number of cells can reduce switching losses. However, because the number of series-connected power devices increases, it is a trade-off between switching losses and conduction losses. This is related to the basic specification in section 3.1, and is an issue for future study. Additionally, if the basic specification is modified, another loss reduction method can be implemented in a different circuit topology. Accordingly, an efficiency of 99.26% at 100 kW output has been reported for a Dual-Active-Bridge (DAB) [43].

Furthermore, there is a literature report [12] on a new circuit topology for motor drive with 3 phase HEECS inverter, in which only the loss of the inverter part is examined, and it showed over 99.5% efficiency. However, to improve the efficiency of the motor drive system, it is necessary to reduce the loss of the inverter as well as that of the motor itself. Future studies for a new topology are still needed to improve the efficiency of a system.

5. Conclusions

This study outlines the latest developments of high efficiency DC-AC power conversion from the perspective of engineering science. Many literatures on high efficiency DC-AC inverters exceeding 99.5% have been published; however, it has been pointed out that the accuracy of the measurement method is important when the efficiency increases. The authors reviewed the literatures on significantly high-efficiency inverters published by the authors' group, and outlined the optimization procedure of loss minimization using a HEECS inverter with SiC and GaN devices. The highest efficiency is 99.83% using SiC devices. Finally, this study discusses the future challenges for high efficiency, such as the analysis on the device output capacitance *Coss* and total system conduction resistance, and the investigation of new circuit topologies.

The development of new devices with larger dielectric breakdown strength is expected in the future, leading to the development of higher efficiency inverters as the conduction losses in power devices are highly dependent on this physical constant of the WBG material [44].

Acknowledgment

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Control Scheme for the Lagging Power Factor Operation of a Single-Phase Grid-Connected Inverter Using an Unfolding Circuit

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ABSTRACT A single-phase grid-connected inverter with an unfolding circuit typically consists of a first-stage dc/dc converter, which generates fully rectified sinusoidal waveforms, and a second-stage unfolding inverter, which switches every 180° of the line frequency waveform. This converter exhibits low switching loss and high efficiency, and the operating principle of the unfolding inverter typically includes synchronous voltage and current. However, limited studies have focused on the operation of inverters with power factor (PF) less than unity. Such operations often result in large overshoots and oscillations in the output voltages. To address this problem, we proposed a novel control scheme that enables leading PF operation without additional circuitry and overcomes the aforementioned limitations in the previous literature. Thus, this paper describes a novel control scheme that enables lagging PF operation. Notably, for a lagging PF, a phenomenon in which the dc voltage inevitably increases immediately after unfolding is known to occur, and herein, this phenomenon is used in reverse to rapidly decrease the dc current. Consequently, we develop a method to land the circuit variables at normal mode steady-state value by using reverse-polarity pulse width modulation (PWM)/forward-polarity PWM combination of the unfolding inverter and a virtual PWM inverter in the proposed controller. The control method is validated using simulations and experiments, and it is found to facilitate the four-quadrant operation of the unfolding inverter.

INDEX TERMS High efficiency, power factor, lagging power factor, single-phase grid-connected inverter, unfolding inverter, reverse- polarity PWM, virtual PWM inverter, four-quadrant operation.

I. INTRODUCTION

Typically, an inverter with an unfolding circuit consists of a first-stage dc/dc converter, which generates a fully rectified sinusoidal voltage or current waveform, and a second-stage unfolding inverter, which switches every 180° of the line frequency waveform and generates a sinusoidal voltage or current [1].

Notably, initial research on unfolding inverters primarily focused on the isolation and miniaturization of passive components [1], [2], [3], [11], [12], [13], [14], [15], [16], [17], [18]. However, leveraging low switching losses of unfolding inverters, several studies have now focused on realizing inverters with low total losses [4], [5], [6], [7], [20], [38].

One example of an inverter application is a grid-connected inverters used for photovoltaic power generation and other distributed energy generations. Grid-connected inverters are often required to provide reactive power as a system support functions for grid stabilization [19]. Although the grid code is known to differ across countries, a system may be required to output reactive power that is 0.484 times the rated real power with leading or lagging power factor (PF), as depicted in Fig. 1 [19]. This corresponds to PF of 0.9. In summary, providing reactive power from a lagging PF of 0.9 to a leading PF of 0.9 is sufficient in practice.

In unfolding inverters, inverter devices are switched every half cycle in synchronization with the voltage zero crossing [1], [6], [7]. Thus, for a unity PF, synchronous voltage and

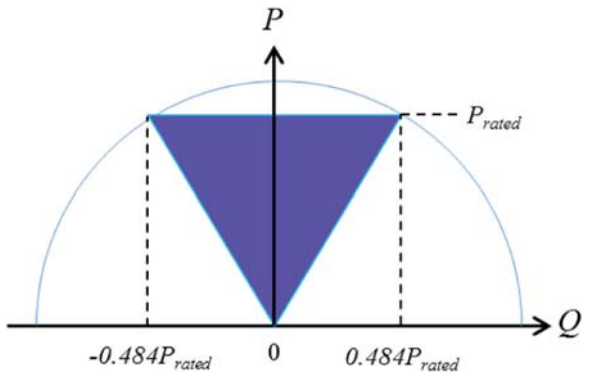


FIGURE 1. Reactive power requirements for distributed energy resources [19].

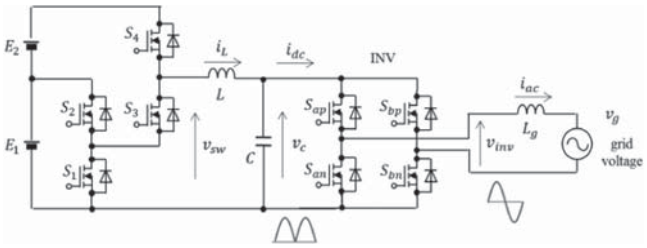


FIGURE 2. Grid-connected inverter based on the HEECS.

TABLE 1. Relationship Between DC/DC Converter Switch States and Output Voltage

S_1	S_2	S_3	S_4	v_{sw}
ON	OFF	ON	OFF	0
OFF	ON	ON	OFF	E_1
OFF	ON	OFF	ON	$E_1 + E_2$

current zero crossing occur in unfolding inverters. By contrast, for a non-unity PF, the voltage transient response becomes oscillatory after unfolding [6], [20]; therefore, appropriate control is required.

However, only limited studies have focused on the non-unity PF control of unfolding inverters. Some have incorporated external circuits to handle reactive power [8], [9], while some others proposed quasi-sinusoidal current reference, however, the output has very large harmonic contents [10].

In [7], the authors used an unfolding inverter with a multilevel chopper called a high efficiency energy conversion system (HEECS) in the first dc/dc converter. Later, for a leading PF operation from the grid-connected inverter perspective (lagging PF from the grid perspective), a new method satisfying the International Electrotechnical Commission (IEC) harmonics regulation based on control alone while maintaining 99.75% class efficiency was proposed, and experimentally demonstrated [39]. However, for a lagging PF from the inverter perspective, no studies have satisfied the requirements of harmonic regulation while maintaining high efficiency through control alone. Min et al. [35] and Han et al. [36] operated an inverter in the pulse width modulation (PWM) mode for a time period before and/or after voltage zero crossing, which increased switching loss as well and decreased efficiency. Generally, when an unfolding inverter is operated with a lagging PF, a phenomenon in which the dc capacitor voltage inevitably increases immediately after the voltage zero crossing is known to occur, is generally difficult to control. Here, we propose the reverse use of this phenomenon. First, the inverter is changed to the freewheeling mode to rapidly decrease the dc inductor current. Next, the dc capacitor voltage is decreased using reverse/regular-polarity PWM to suppress transients, and the circuit returns to a steady-state. We analyze these control operations in detail, and finally, experiments demonstrate that the HEECS circuit can be operated in a lagging PF mode with high efficiency while the harmonics remain within IEC limits.

The remainder of this paper is organized as follows. Section II reviews the HEECS circuit and its waveforms. In addition, the control method DBCCL+VC is described [39]. Section III describes the problem with the lagging PF operation of an unfolding inverter and proposes a new control scheme to solve this problem. Section III-A describes dc voltage rise after unfolding. Section III-B proposes a new control method based on this phenomenon. In addition, Section III-C proposes a transient response improvement. Section IV presents the effectiveness of the proposed control scheme using simulations and experiments. Section V presents comparison with conventional schemes. Finally, Section VI concludes the paper.

II. CONTROL PRINCIPLE OF AN HEECS INVERTER

A. HEECS INVERTER OPERATION [6]

Fig. 2 depicts an HEECS-based inverter circuit that is connected to the grid through an ac inductor [6], [21], [24].

Note that the multilevel dc/dc converter consists of switching devices S_1, S_2, S_3, and S_4 as well as an LC filter. Table 1 summarizes the relationships between the switch states and outputs of the switching network v_{sw}.

If the voltage command to the dc/dc converter is smaller than E_1, S_1 and S_2 operate in PWM mode. However, if the voltage command is larger than E_1 and smaller than $E_1 + E_2$, S_2 is always ON; moreover, S_3 and S_4 operate in PWM mode. The dc/dc converter is controlled such that the capacitor voltage v_c follows the fully rectified sinusoidal reference voltage. The unfolding inverter consists of switching devices S_{ap}, S_{an}, S_{bp}, and S_{bn}. It switches every 180° electrical degrees of the line frequency waveform. The inverter output voltage v_{inv} is also a sinusoidal waveform. The voltage waveforms for the circuit in Fig. 2 are shown in Fig. 3.

B. CONTROL LAWS

1) DIGITAL CONTROL MODEL

Fig. 4 presents the equivalent circuit of an HEECS inverter [20], [21]. The resonance frequency of the LC filter is on the order of kilohertz, which is considerably higher than the line-

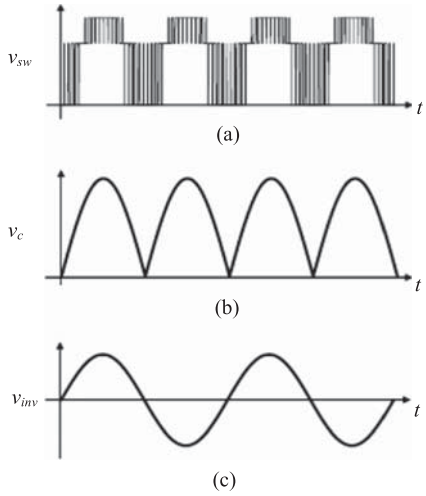


FIGURE 3. Voltage waveforms of the HEECS: (a) dc/dc converter switching circuit output voltage, (b) dc capacitor voltage, (c) inverter output voltage.

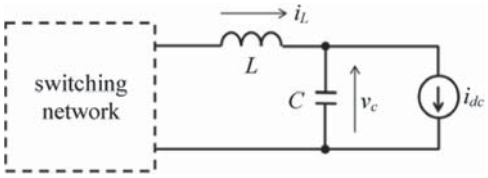


FIGURE 4. Equivalent circuit of the HEECS.

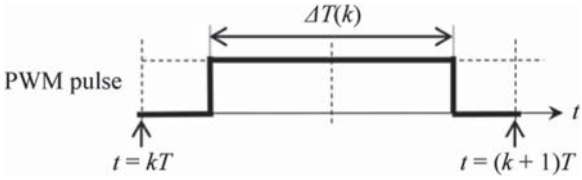


FIGURE 5. PWM pulse waveform.

frequency of 50 or 60 Hz. Furthermore, the sampling control frequency of the dc/dc converter (20 kHz) is high. The ac side transient phenomena are considerably slower than those on the dc side. Thus, the ac output circuit of the inverter is replaced by a dc current source i_{dc}. The circuit equation [25], [26] for the equivalent circuit in Fig. 4 is:

$$\frac{\mathrm{dx}}{\mathrm{dt}} = Ax(t) + B_1 u(t) + B_0 i_{dc} \tag{1}$$

where

$\mathrm{x}(t) = \begin{bmatrix} v_c(t) \\ i_L(t) \end{bmatrix}$, $u(t)$ = output of switching network

$$\mathrm{A} = \begin{bmatrix} 0 & 1/C \\ -1/L & 0 \end{bmatrix},\ B_1 = \begin{bmatrix} 0 \\ 1/L \end{bmatrix},\ B_0 = \begin{bmatrix} -1/C \\ 0 \end{bmatrix}$$

The voltage pulse of the dc chopper is assumed to be centered at the sampling time, as shown in Fig. 5. The width is defined as $\Delta T(k)$ during the sampling period (kT to $(k+1)T$). Consequently, the sampled-data model [25], [26] of (1) is

$$\mathrm{x}[k+1] = Fx[k] + G_1 \Delta T[k] + G_0 i_{dc}[k]$$

$$\mathrm{F} = e^{AT} = \begin{bmatrix} F_{11} & F_{12} \\ F_{21} & F_{22} \end{bmatrix},\ G_1 = e^{AT/2} B_1 E = \begin{bmatrix} g_{11} \\ g_{12} \end{bmatrix}$$

$$G_0 = A^{-1}\left(e^{AT} - I\right) B_0 = \begin{bmatrix} g_{01} \\ g_{02} \end{bmatrix} \tag{2}$$

where F can be expressed as:

$$F = e^{AT} = \begin{bmatrix} \cos \omega_n T & \sqrt{\frac{L}{C}} \sin \omega_n T \\ -\sqrt{\frac{C}{L}} \sin \omega_n T & \cos \omega_n T \end{bmatrix}$$

$$\omega_n = \frac{1}{\sqrt{LC}}$$

The capacitor voltage v_c can be controlled in two ways: deadbeat voltage control law (DBVCL) [6], [20] and deadbeat current control law plus voltage control loop (DBCCL + VC) [22], [23], which have been previously compared in [39]. The DBVCL has higher gain and larger transient response than DBCCL + VC; thus only DBCCL + VC is introduced here.

2) DBCCL

The pulse width ΔT(k) of DBCCL is decided such that the inductor current $i_L(\mathrm{k}+1)$ at the next sampling instant $(k+1)T$ matches the current reference $i_{Lref}(k+1)$ [22], [23], [24].

Considering the second row of (2), we obtain

$$i_L(k+1) = F_{21} v_c(k) + F_{22} i_L(k) + g_{12} \Delta T(k) + g_{02} i_{dc}(k) \tag{3}$$

and solving for $\Delta T(k)$ after replacing $i_L(k+1)$ with i_{Lref} yields DBCCL as

$$\begin{aligned} \Delta \mathrm{T}(k) &= \left(i_{Lref} - F_{21} v_c(k) - F_{22} i_L(k) - g_{02} i_{dc}(k)\right) / g_{12} \\ &= \left[-\frac{F_{21}}{g_{12}} \quad -\frac{F_{22}}{g_{12}}\right] x(k) + \frac{1}{g_{12}} i_{Lref} - \frac{g_{02}}{g_{12}} i_{dc}(k) \\ &= K_2 x(k) + \frac{1}{g_{12}} i_{Lref} - \frac{g_{02}}{g_{12}} i_{dc}(k) \end{aligned} \tag{4}$$

The first, second, and third terms in (4) represent the state feedback, reference input, and disturbance feed-forward compensation, respectively. Furthermore, a voltage control loop is added as an outer control loop, as discussed below.

3) DBCCL + VC LOOP

A VC loop is added as an outer control loop around the current control, as shown in Fig. 6. Current reference i_{Lref} is generated using a proportional controller, as follows:

$$i_{Lref} = K_{pv}\left(v_{cref} - v_c\right) \tag{5}$$

The combination of (4) and (5) is designated as DBCCL + VC. For a more detailed analysis of the control system that applies DBCCL + VC, see Appendix B of [39].

Ac current control is also required for grid-connected inverters. A control block diagram is presented in Appendix A.

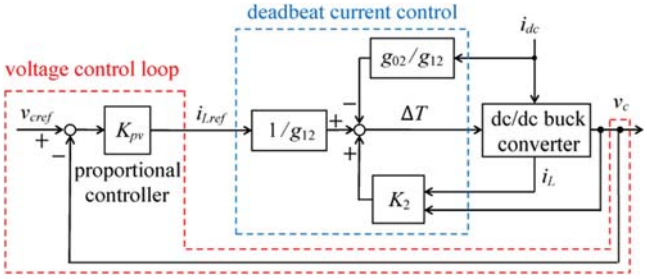


FIGURE 6. Control block diagram of DBCCL + VC.

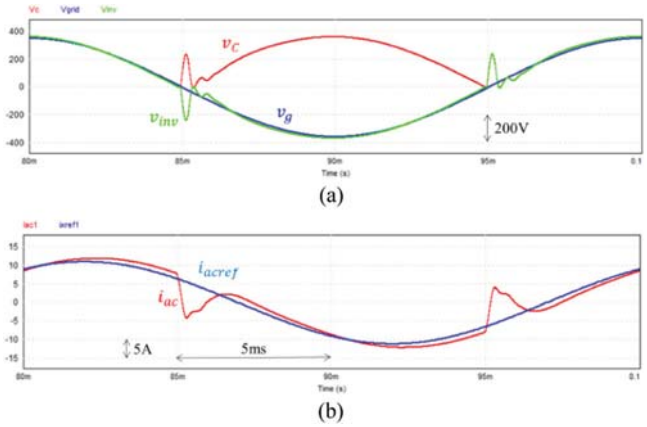


FIGURE 7. Simulation waveforms of an HEECS controlled by DBCCL + VC in lagging PF operation (a) dc capacitor voltage v_c, inverter output voltage v_{inv}, and grid voltage v_g, (b) grid current reference i_{acref}, and grid current i_{ac}.

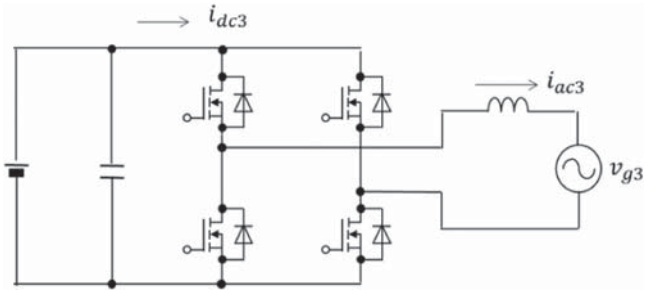


FIGURE 8. Grid-connected inverter using a conventional PWM voltage source inverter.

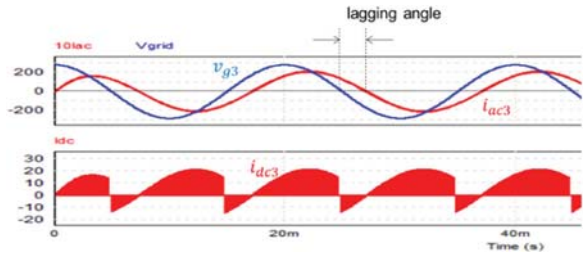


FIGURE 9. Simulated waveforms of the conventional PWM grid-connected voltage source inverter in lagging PF operation.

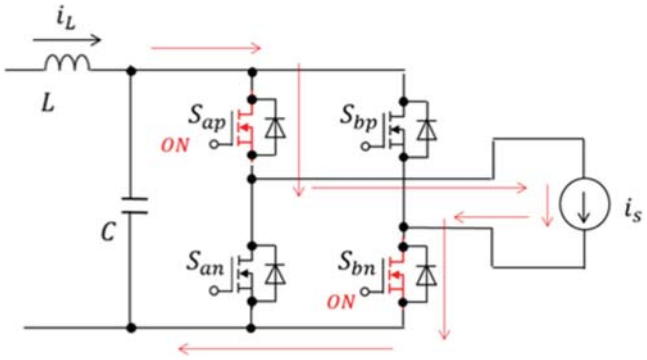


FIGURE 10. Current path before voltage zero crossing in the lagging PF mode.

III. PROPOSED CONTROL METHOD AFTER VOLTAGE ZERO CROSSING OF AN HEECS INVERTER WITH LAGGING PF OPERATION

A. PROBLEM OF LAGGING PF OPERATION IN AN HEECS INVERTER AND ITS ANALYSIS

Fig. 7 presents the simulated waveforms of an HEECS controlled by DBCCL + VC during lagging PF operation. The inverter is simply unfolded every 180°. Circuit conditions are real power reference $P_{ref} = 1600$ W, reactive power reference $Q_{ref} = -1200$ var, PF of 0.8, and a grid voltage of 280 V_{rms}, 50 Hz. Immediately after unfolding, the dc capacitor voltage rapidly increases. The voltage controller attempts to regulate the dc voltage; however, its response is extremely fast, causing oscillations. Accordingly, the grid current is highly distorted. The total harmonic distortion (THD) of the grid current is 29.8%.

The following section presents analysis of the phenomenon after voltage zero crossing. For reference, the conventional PWM voltage source inverter connected to the grid is displayed in Fig. 8, and the typical simulated waveforms of the grid voltage v_{g3}, ac current i_{ac3}, and dc current i_{dc3} of the circuit with lagging PF under ideal conditions are depicted in Fig. 9. In the PWM inverter waveforms presented in Fig. 9, the dc current changes from positive to negative at the voltage zero crossing owing to lagging PF. Because the voltage zero crossing occurs twice during every period of the ac line voltage, the voltage changes from negative to positive at a 0° electrical angle and from positive to negative at 180°. Here, the 180° case is discussed in detail.

Fig. 10 depicts the current path of HEECS just before the voltage zero crossing (just before unfolding) during lagging PF operation. The current flows through the devices S_{ap} and S_{bn}. At the voltage zero crossing, the unfolding control circuit provides ON gate signals to the devices S_{an} and S_{bp}. Fig. 11 depicts the current path immediately after the voltage zero crossing (immediately after unfolding). Currents pass through the diode part of S_{an} and the diode part of S_{bp}, and the dc capacitor is fed from the right by the current $-i_{dc}$, whose magnitude is equal to the ac current at that point. By contrast, the dc capacitor is fed from the left by the dc inductor current

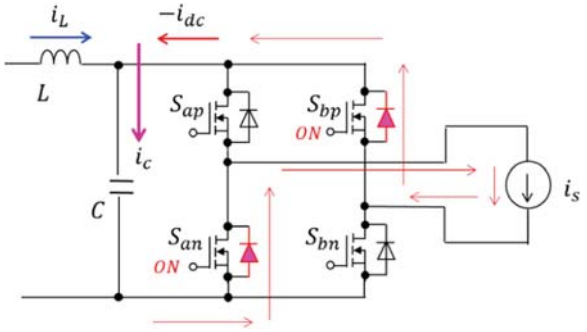


FIGURE 11. Current path just after voltage zero crossing in the lagging PF mode.

i_L. Currents flow into the capacitor from both the left and right sides, and the capacitor voltage increases sharply. The voltage rise depicted in Fig. 7 originates from this circuit behavior, and the voltage increase after unfolding is inevitable. This makes it difficult to control unfolding inverters during lagging PF operation; however we attempted to use this phenomenon in reverse. The following subsection describes the control sequence immediately after unfolding.

B. PROPOSED CONTROL SEQUENCE AFTER VOLTAGE ZERO CROSSING

Fig. 12 presents the control sequence timing chart after voltage zero crossing. As shown in Fig. 12, unfolding occurs at t_0. In Section S1, the circuit is as shown in Fig. 11, the dc capacitor voltage sharply increases. In Section S2, after t_1, the inverter is operated in the freewheeling mode, as shown in Fig. 13. One purpose of this mode is to prevent the large dc voltage from affecting the ac current. Another purpose of this mode is to control the dc inductor current independently of ac side. In Fig. 13, ON gate signals are provided to the devices in the upper arms; however, such ON gate signals can be assigned to the devices in the lower arms. In Fig. 12, unfolding is executed for only one cycle; however, unfolding can be continued for two cycles to rapidly reduce the dc inductor current in Section S2.

Fig. 14 presents the equivalent circuit of the dc/dc converter in section S2. For example, when the switching frequency is 20 kHz, the switching circuit in Fig. 14 can control the dc inductor current by outputting pulses with a width ΔT in the range of 0–50 μs as shown in Fig. 5 for each cycle.

In the first cycle in Section S2, the circuit outputs a pulse with $\Delta T = 0$, corresponding to the minimum voltage, thus decreasing the dc inductor current rapidly by applying a voltage difference between the switching circuit output and the boosted dc capacitor voltage. The control objective of the Section S2 is to decrease the dc inductor current i_L from the i_{ac} value at the start of unfolding to the $-i_{ac}$ value, the same absolute value as in the reverse polarity. When the dc inductor current i_L approaches $-i_{ac}$, the circuit outputs partial duty ΔT_2 so that i_L matches $-i_{ac}$ at the final time t_3 of Section S2.

Then, in Section S3 of Fig. 12, the inverter is operated by a combination of the reverse-polarity PWM and regular-polarity PWM modes. The reverse-polarity PWM mode outputs PWM pulses of the opposite polarity as the output polarity of the unfolding inverter in the 180° section. The regular-polarity PWM mode outputs PWM pulses of the same polarity as the output polarity of the unfolding inverter in the 180° section. The current path in the reverse-polarity PWM mode is shown in Fig. 15. For the original polarity of the unfolding inverter, ON gate signals are assigned to S_{an} and S_{bp}. In the reverse-polarity PWM mode, ON gate signals are assigned to S_{ap} and S_{bn}. Current i_{dc} flows to the right side of the capacitor. In addition dc inductor current i_L flows to the left side of the capacitor because the current polarity is already reversed. Therefore, the capacitor voltage decreases rapidly. When the capacitor voltage approaches the desired value, reverse/regular-polarity PWM is used as needed. In the regular-polarity PWM, the inverter outputs the original polarity. The current path of regular-polarity PWM is shown in Fig. 16. Note that the direction of the dc inductor current is opposite to that immediately after unfolding described in Fig. 11. Inverter gate pattern and capacitor voltage waveform in the reverse-polarity PWM mode are shown in Fig. 17. Here, ΔU is pulse width of the unfolding inverter output pulse. Current flows out both to the left and right directions during the section $[t_{u1}, t_{u2}]$. To the right direction, current $i_{dc} = +i_{ac}$ flows. Current i_L flows to the left direction. The dc inductor current i_L is controlled to reach abs (i_{ac}) at the end of Section S2. Therefore, the slope of the capacitor voltage during $[t_{u1}, t_{u2}]$ is as follows:

$$dv_c/dt = -2 * \text{abs}\,(i_{ac})\,/\text{C}$$

By contrast, sections $[t_{u0}, t_{u1}]$ and $[t_{u2}, t_{u3}]$ are in the freewheeling mode. Because $i_{dc} = 0$, the slope of the capacitor voltage in these sections is

$$dv_c/dt = -\text{abs}\,(i_{ac})\,/\text{C}$$

The average slope of the capacitor voltage over the entire section $[t_{u0}, t_{u3}]$ is as follows:

$$\left(-2\frac{\Delta U}{T}\text{abs}\,(i_{ac}) - \frac{T-\Delta U}{T}\text{abs}\,(i_{ac})\right)/C$$

By adjusting ΔU from zero to T, the slope can be adjusted from $-$abs(i_{ac})/C to -2abs(i_{ac})/C.

Fig. 18 presents the inverter gate pattern and capacitor voltage waveform in the regular-polarity PWM mode. We assume that the sign of ΔU is positive for reverse-polarity PWM, and negative for regular-polarity PWM. In section $[t_{u1}, t_{u2}]$, the input and output currents for the capacitor are balanced; thus the capacitor voltage is constant. However, sections $[t_{u0}, t_{u1}]$ and $[t_{u2}, t_{u3}]$ are in the freewheeling mode, and the slope of the capacitor voltage in these sections is as follows:

$$dv_c/dt = -\text{abs}\,(i_{ac})\,/\text{C}$$

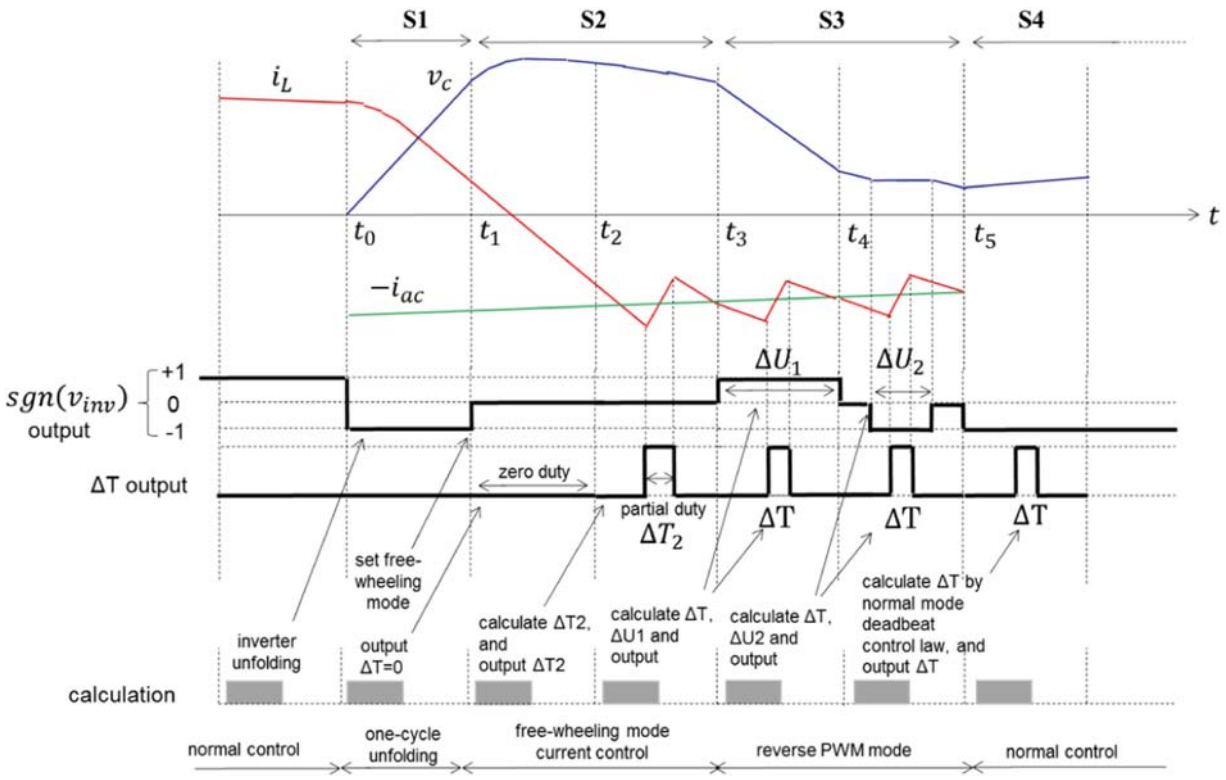


FIGURE 12. Timing chart after voltage zero crossing.

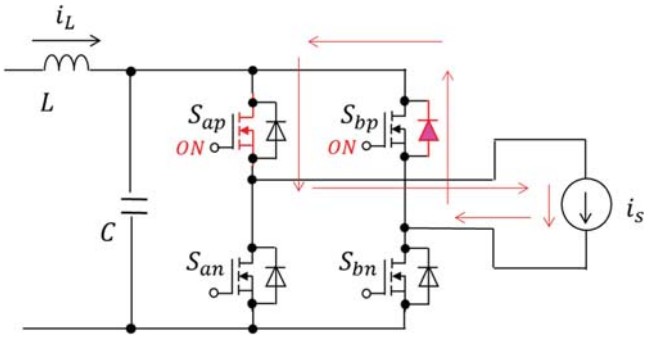


FIGURE 13. Freewheeling mode for Section S2.

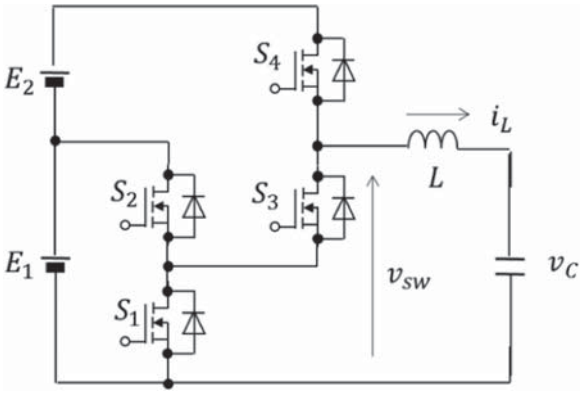


FIGURE 14. Equivalent circuit of the dc/dc converter during Section S2.

The average slope of the capacitor voltage over the entire section $[t_{u0}, t_{u3}]$ is as follows:

$$-\frac{T+\Delta U}{T}\text{abs}\left(i_{ac}\right)/C$$

By adjusting ΔU from zero to −T, the slope of the capacitor voltage can be adjusted from −abs(i_{ac})/C to zero.

Table 2 summarizes the inverter pulse pattern, capacitor voltage behavior, and sign of ΔU for various modes, including the reverse-polarity PWM mode, no-pulse mode, regular-polarity PWM mode, and regular-polarity whole- pulse mode. By adjusting ΔU from T to −T, the slope of the capacitor voltage can be continuously adjusted.

In practice, the capacitor voltage and dc inductor current are governed by (2). In other words, this system controls two outputs, namely the capacitor voltage and dc inductor current, using two inputs, ΔT and ΔU, during Section S3, as illustrated in Fig. 19. To make the capacitor voltage and dc inductor current reach the target values at return to the normal mode, we need to solve for ΔU and ΔT. Appendix B describes in detail the equation with ΔU and ΔT. In the final cycle of Section S3 in Fig. 10, we aim for a smooth transition to the normal mode of Section S4 by using ΔU and ΔT obtained by solving this equation.

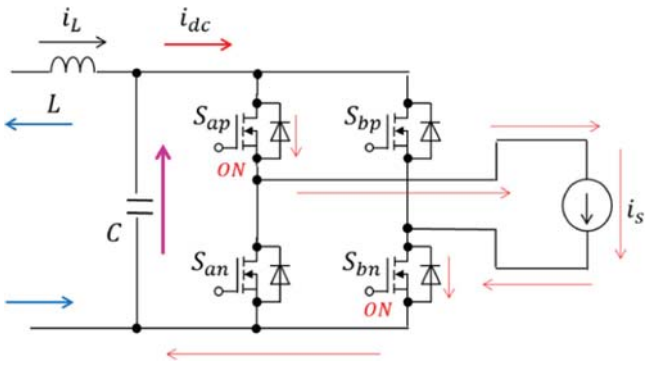


FIGURE 15. Current path of the reverse-polarity PWM mode in Section S3.

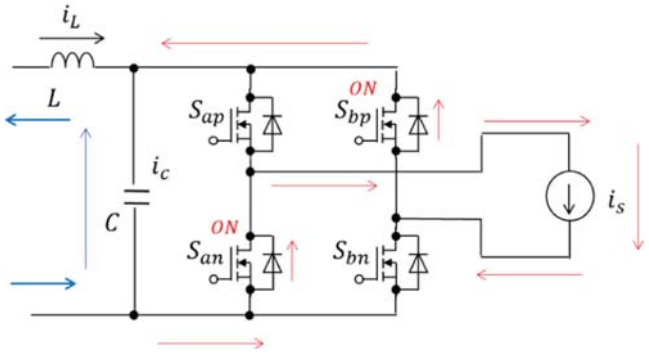


FIGURE 16. Current path of the regular-polarity PWM mode in Section S3.

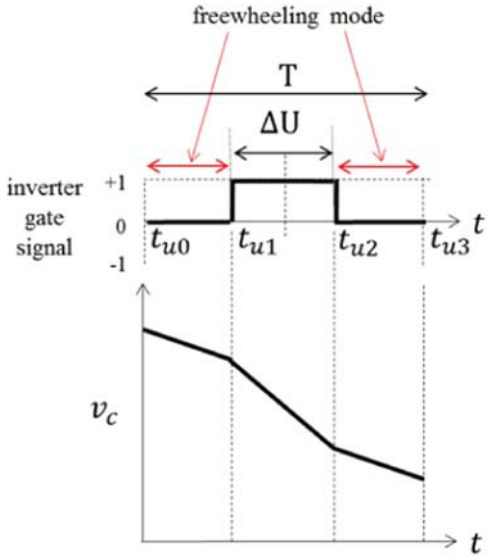


FIGURE 17. Waveforms in the reverse-polarity PWM mode.

C. IMPROVEMENT IN TRANSIENT RESPONSE AFTER UNFOLDING

1) TRANSIENT RESPONSE

Fig. 20 presents an example of the simulation results obtained using the control sequence proposed in Section III-B. The

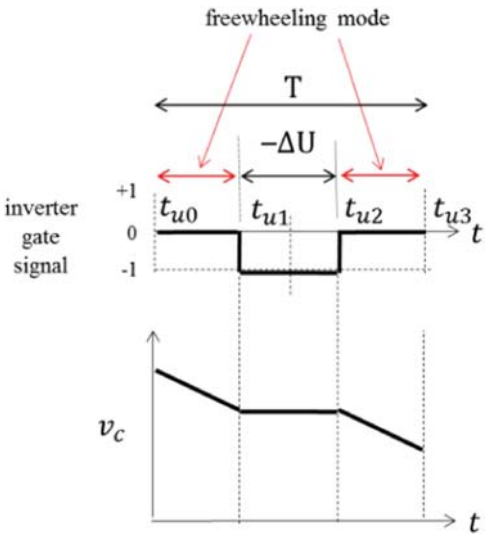
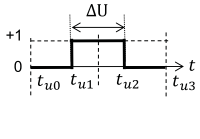
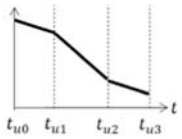
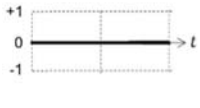
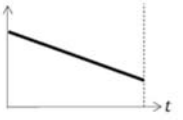
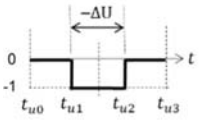
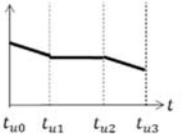
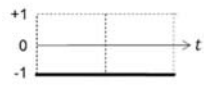


FIGURE 18. Waveforms in the regular-polarity PWM mode.

TABLE 2. Relation Between Inverter Pulse Pattern and Slope of Capacitor Voltage

mode	inverter pulse pattern	capacitor voltage behavior	ΔU
reverse-polarity PWM mode			0<ΔU≦T
no-pulse mode			ΔU = 0
regular-polarity PWM mode			−T<ΔU<0
regular-polarity whole-pulse mode			ΔU = −T

circuit conditions are $P_{ref} = 1600$ W, $Q_{ref} = -1200$ var, PF = 0.8, and $V_g = 280$ V_{rms}. At the end of Section S3 in Fig. 12, at $t = t_5$, the capacitor voltage reference v_{cref} and dc inductor current reference i_{Lref} in Fig. 6 are used as the target values for the dc capacitor voltage and dc inductor current, respectively.

In Fig. 20, unfolding is executed over two cycles in Section S1, and the capacitor voltage v_c increases rapidly as shown in Fig. 11. In Section S2, freewheeling mode is conducted for three cycles. The dc inductor current i_L rapidly decreases and reaches the target value $-\text{abs}(i_{ac})$ at the end of Section S2. Section III presents the reverse-polarity PWM, and the capacitor voltage is decreased as intended.

FIGURE 19. Input/output relation in Section S3.

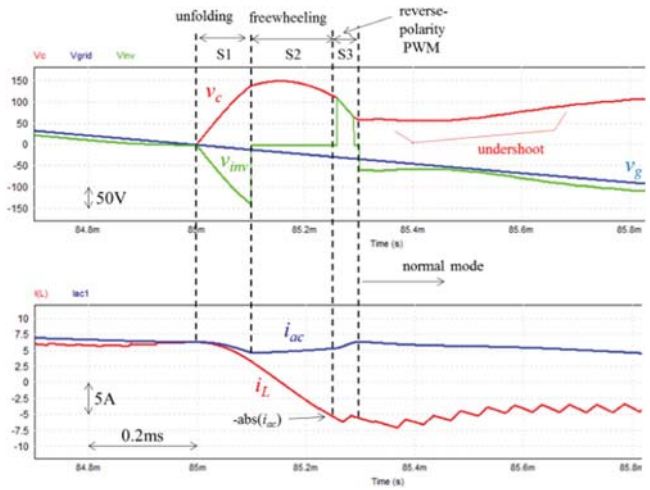


FIGURE 20. Example of simulation result.

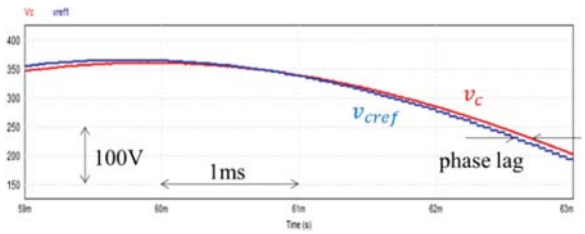


FIGURE 21. Simulation example: dynamics between v_{cref} and v_c. (Conditions are the same as those for Fig. 20).

However, a small undershoot is observed in the capacitor voltage waveform after returning to the normal mode in Section S4. Hereafter, this phenomenon is discussed. In Fig. 6, a relationship can be established between the current reference i_{Lref} and the current value i_L. The transfer function from i_{Lref} to i_L is as follows:

$$i_L/i_{Lref} = 1/z$$

as calculated in (A2-3) of Appendix A in [39].

In addition, a dynamic relationship exists between the capacitor voltage reference v_{cref} and capacitor voltage v_c. Its transfer function is as follows:

$$\frac{v_c}{v_{cref}} = \frac{K_{pv}g_r\,(z+1)}{z^2 + \left(K_{pv}g_r - 1\right)z + K_{pv}g_r}$$

Although i_L and v_c follow the references i_{Lref} and v_{cref}, respectively, they do not exactly match, and a phase lag exists. Fig. 21 shows a simulation example, in which a phase lag is observed between v_{cref} and v_c.

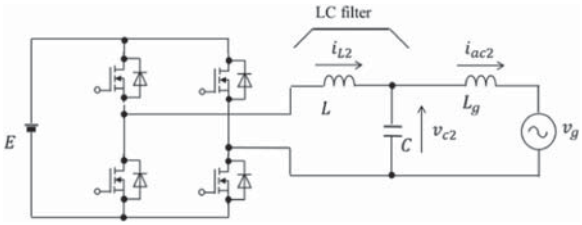


FIGURE 22. Circuit diagram of the proposed virtual PWM inverter.

Therefore, the target values to realize a smooth transition to the normal mode without transients should not be v_{cref} and i_{Lref}, which were adopted in Fig. 20, but should be the normal mode steady-state values of v_c and i_L at the end of Section S3. However, the controller of this system controls the unfolding sequence and thus cannot predict the normal mode steady-state values.

2) VIRTUAL PWM INVERTER

To solve this problem, we propose a virtual PWM inverter, and a circuit diagram is shown in Fig. 22. The differences with the HEECS circuit diagram in Fig. 2 are as follows: (a) the LC filter in Fig. 2 is moved to the ac side in Fig. 22, and (b) the PWM function of the dc/dc converter in Fig. 2 is moved to the PWM inverter in Fig. 22. To distinguish it from a real HEECS circuit, the capacitor voltage, inductor current, and ac current of the virtual circuit are denoted as v_{c2}, i_{L2}, and i_{ac2}, respectively. The discrete-time equation of this virtual circuit is the same as in (2), except that i_{dc} changes to i_{ac2}. The equation is as follows:

$$x_2\,[k+1] = F x_2\,[k] + G_1 \Delta T_2\,[k] + G_0 i_{ac2}\,[k] \qquad (6)$$

where

$$x_2\,(k) = \begin{bmatrix} v_{c2}\,(k) \\ i_{L2}\,(k) \end{bmatrix}$$

ΔT_2 is the pulse width of the virtual PWM inverter and can be both positive and negative. Therefore, the same structure control law, DBCCL + VC, described in (4) and (5), can be used to control the capacitor voltage v_{c2}, and the same structure control law can be used to control the ac current i_{ac2}. The virtual PWM inverter does not exhibit complex phenomena related to unfolding; thus, the circuit exhibits a smooth waveform, even after the voltage zero crossing.

Fig. 23 shows the control block diagram, which includes both the real HEECS inverter and the virtual PWM inverter. In Fig. 23, part of the virtual PWM inverter + LC filter is realized by calculating (6) within the controller. Part of the virtual grid-tie circuit is calculated using a simple discrete equation.

$$i_{ac2}\,(k+1) = i_{ac2}\,(k) + \frac{T}{L_g}\left(v_{c2} - v_g\right) \qquad (7)$$

This equation is deduced from the circuit equation of the virtual grid-tie circuit illustrated in Fig. 24 by simple discretization. The ac current reference for the current controller

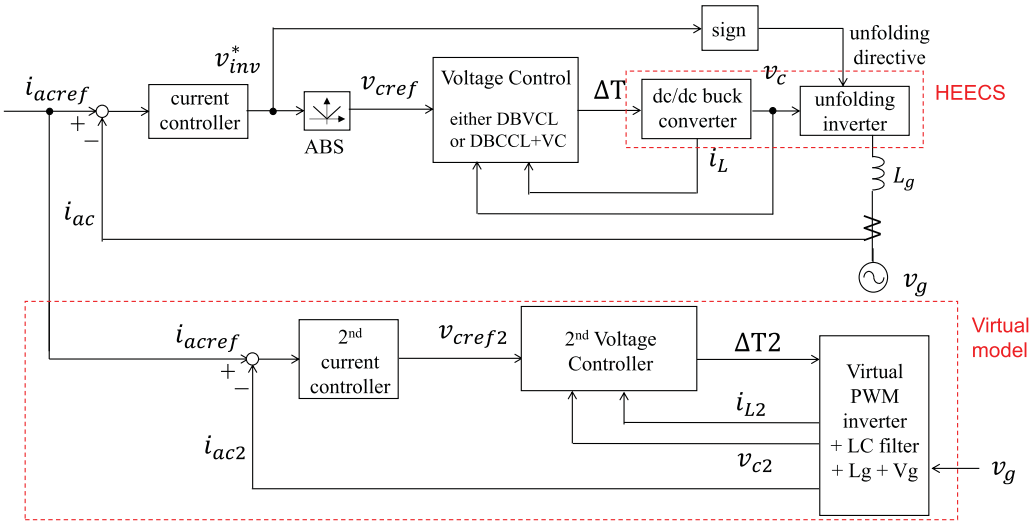


FIGURE 23. Control block diagram including both the real model and virtual model.

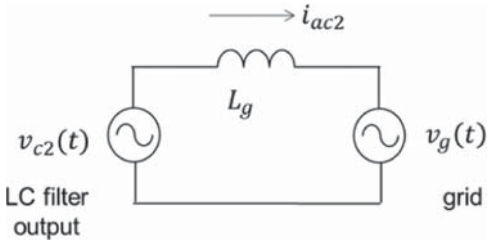


FIGURE 24. Circuit diagram of the virtual grid-tie circuit.

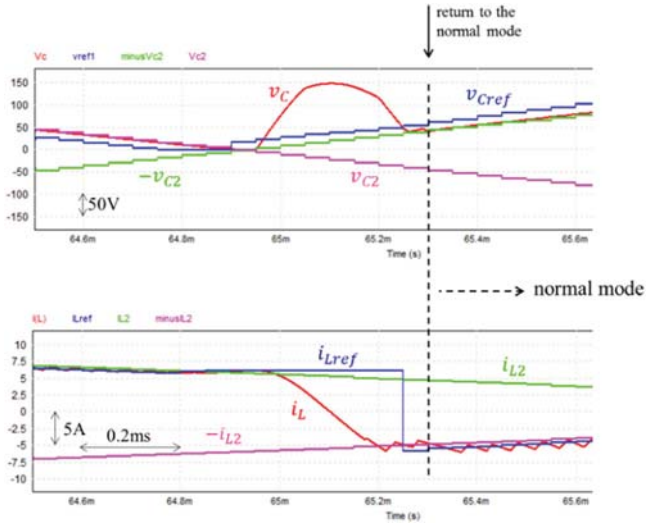


FIGURE 25. Simulation result when the target values are determined from the virtual circuit.

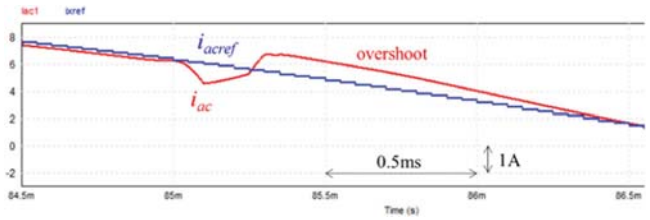


FIGURE 26. Simulation result of ac current (the same condition as Fig. 25).

i_{acref} is common for the upper real circuit and the lower virtual circuit in Fig. 23. A second current controller is used to control the virtual ac current i_{ac2}. In addition, a second voltage controller is used to control the virtual PWM inverter capacitor voltage. The structure and gains of the second current controller and voltage controller are the same as those of the real controllers. We propose adopting abs(v_{c2}) and −abs(i_{L2}) from the virtual circuit as target values of the dc capacitor voltage and dc inductor current, respectively, at the end of Section S3 in Figs. 12 and 20.

Note that the circuit parameters in the virtual circuit may differ from those in the real HEECS circuit owing to fabrication errors and age-related deterioration. In addition, numerical errors may accumulate over long time of operations in the virtual circuit. Thus, it is desirable that the variables of the virtual circuit be reset by the values of the corresponding real circuit variables at every specified period to prevent numerical error accumulation.

Fig. 25 shows the simulation results when the target values from the virtual circuit are adopted. At the start of the normal mode, the dc capacitor voltage and dc inductor current land at the target values determined from the virtual circuit, and transients are not observed.

Fig. 26 shows the simulation results of the ac current reference and ac current. A large overshoot can be observed in the ac current. To address this overshoot, another device is required, which is discussed in the next subsection.

3) UNFOLDING TIMING SHIFT

Fig. 27 presents magnified waveforms near the voltage zero crossing. The ac current i_{ac} increases in Sections S2 and S4,

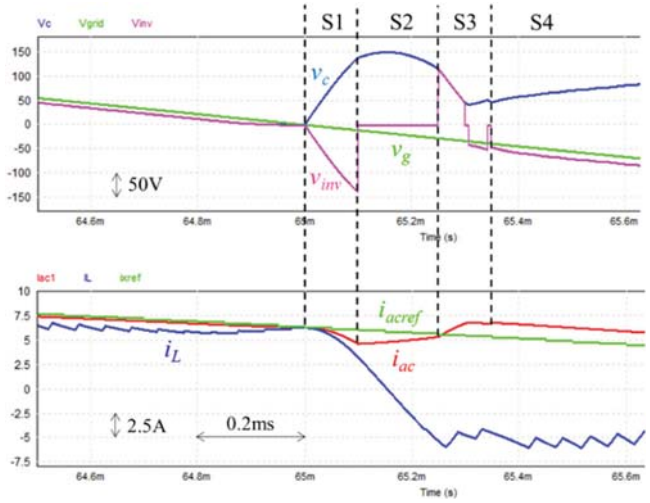


FIGURE 27. Zoomed-in waveforms near the voltage zero crossing.

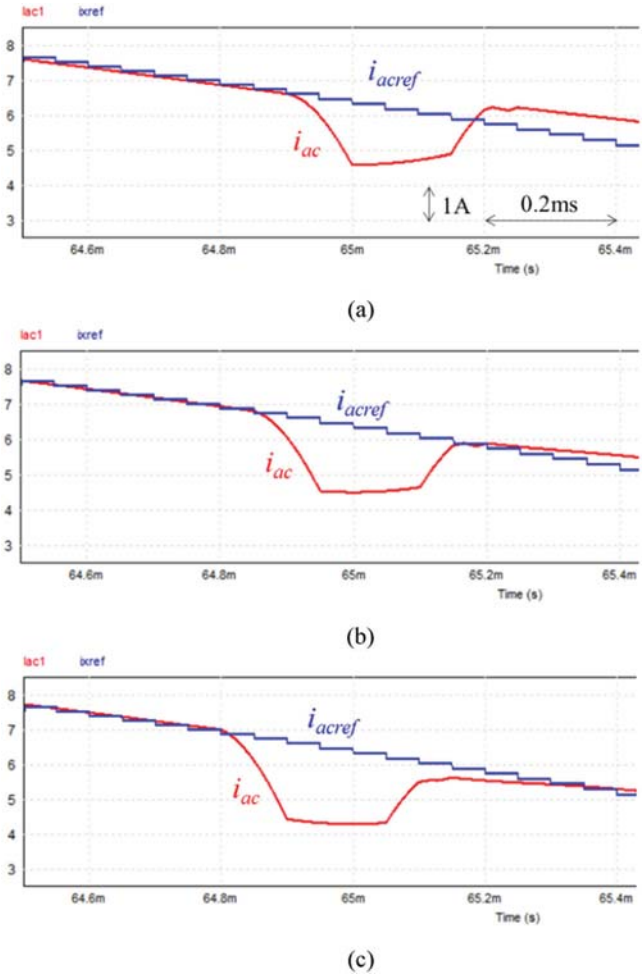


FIGURE 28. AC current waveforms with unfolding timing shift: (a) two-cycle forward, (b) three-cycle forward, and (c) four-cycle forward.

resulting in an overshoot. In Section S3, the inverter voltage is manipulated to decrease the dc capacitor voltage rapidly, and it is natural for the inverter voltage to exceed the grid voltage. So far, we have been unfolding at the voltage zero crossing. Owing to the small phase difference between the inverter and grid voltages, after the inverter voltage crosses zero and becomes negative, the grid voltage also becomes negative. For leading PF operation, after unfolding at the inverter voltage zero crossing, an all-conduction mode occurs, and the dc inductor current is rapidly increased during the all-conduction mode. This means that unfolding at the voltage zero crossing is required for a leading PF operation [39]. However, for lagging PF operation, no specific approach is required for unfolding at the voltage zero crossing. Even if the unfolding timing is shifted, once the ac current is positive during unfolding, the dc capacitor voltage quickly increases, and the control sequence described in Section III-B can be executed.

Therefore, a shift in forward unfolding timing is proposed. A sinusoidal wave observer with the inverter voltage as the input is discussed as follows [39].

$$\begin{bmatrix} \widehat{v_{ix}}(k+1) \\ \widehat{v_{iy}}(k+1) \end{bmatrix} = F_s \begin{bmatrix} \widehat{v_{ix}}(k) \\ \widehat{v_{iy}}(k) \end{bmatrix} + K_{ixy}\left(v_{inv} - \widehat{v_{ix}}\right) \tag{8}$$

where

$$F_s = \begin{bmatrix} \cos\omega T & -\sin\omega T \\ \sin\omega T & \cos\omega T \end{bmatrix}$$

$\widehat{v_{ix}}$ is the estimated value of v_{inv}, and $\widehat{v_{iy}}$ is the estimated value of the orthogonal component. These components in steady-state can be expressed as sinusoidal functions as follows:

$$\widehat{v_{ix}} = V_i \cos(\omega kT + \varphi)$$
$$\widehat{v_{iy}} = V_i \sin(\omega kT + \varphi)$$

A sinusoidal wave that leads the inverter voltage by phase ε can be expressed as

$$\widehat{v_{i\epsilon}} = V_i \cos(\omega kT + \varphi + \varepsilon)$$
$$= \widehat{v_{ix}} \cos\varepsilon - \widehat{v_{iy}} \sin\varepsilon$$

By unfolding at the moment when this waveform crosses zero, the unfolding timing can be shifted forward.

When the switching frequency is 20 kHz, one cycle is 50 μs. Ac current waveforms when unfolding is shifted forward by two cycles (100 μs), three cycles (150 μs), and four cycles (200 μs) are shown in Fig. 28. In three-cycle forward case, ac current reaches the ac current reference exactly; thus three-cycle forward is adopted.

Fig. 29 shows a small zoomed-out ac current waveform with three-cycle forward unfolding shift. This is much better than that shown in Fig. 26; however, a small overshoot is still observed.

As shown in Fig. 30, the current control block diagram, ac current i_{ac} is input to the sinusoidal wave observer, then the orthogonal components are obtained, the d-axis and q-axis

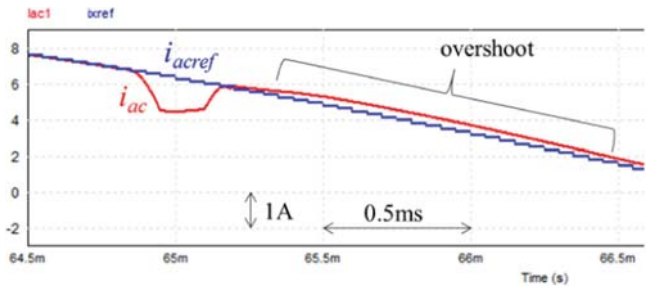


FIGURE 29. AC current waveform with three-cycle forward unfolding timing.

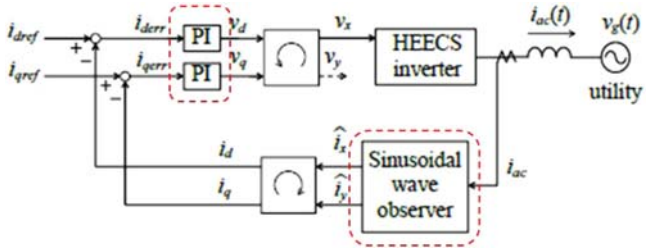


FIGURE 30. Current control block diagram.

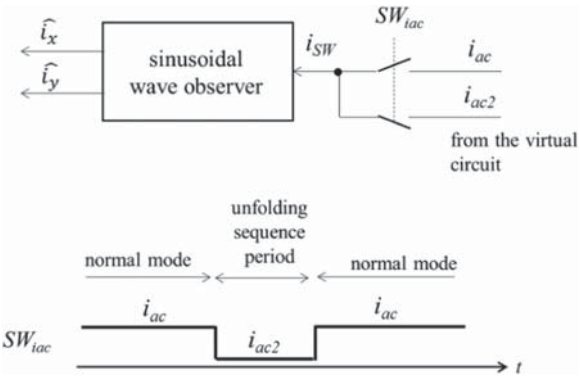


FIGURE 31. AC current signal selection to the sinusoidal wave observer in Fig. 30.

components are calculated, and these are compared with the current references i_{dref} and i_{qref}; the errors are then input to proportional-integral (PI) controllers. After unfolding, the ac current inherently deviates from the ac current reference until the system returns to the normal mode; thus the error is accumulated in the PI controllers. The accumulated errors cause a small overshoot, as shown in Fig. 29.

We propose that during the unfolding control sequence of Sections S1, S2, and S3 in Fig. 12, we provide an ac current signal as if the ac current is controlled sinusoidal. Fig. 31 presents an ac current signal selection block diagram. Here, i_{ac2} is the virtual ac current in Fig. 23. Switch SW_{iac} is connected to the i_{ac2} side during the unfolding control sequence; otherwise, it is connected to the i_{ac} side. Fig. 32 shows the

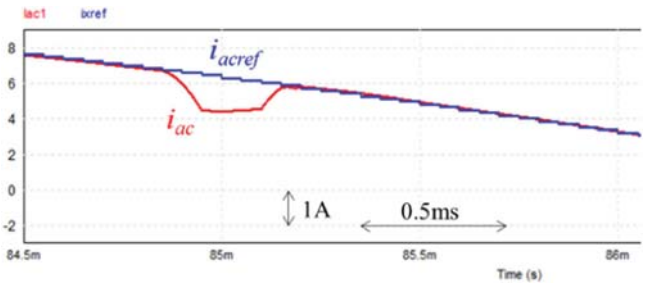


FIGURE 32. Simulation result.

FIGURE 33. Experimental setup.

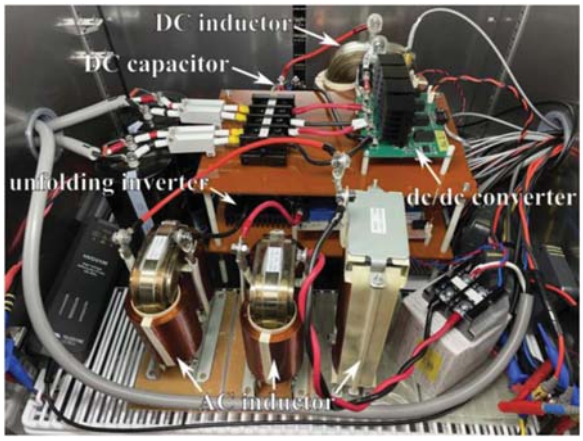


FIGURE 34. Circuit under test.

simulation results when the scheme shown in Fig. 31 is used. The overshoot shown in Fig. 29 is eliminated.

IV. SIMULATION AND EXPERIMENT RESULTS

A. SET-UP

Figs. 33 and 34 present the experimental setup and circuit under testing, respectively. The test circuit is installed in a thermostatic chamber. Table 3 lists the circuit parameters used

TABLE 3. Circuit Parameters

Grid voltage	280 Vrms, 50 Hz
Grid-tie inductor	L_g = 3.77mH (%impedance = 3.01%)
Dc capacitor	C = 8 μF
Dc inductor	L = 2.43 mH
Dc source voltage	E_1 = 250 V, E_2 = 183 V
Dc/dc converter devices	SCT3017AL (Rohm)
Inverter devices	CAS325M12HM2 (Wolfspeed)
Carrier frequency	20 kHz

TABLE 4. List of Equipment

Ac voltage source	NF Corporation: DP060RS
Dc voltage source	Headspring: biATLAS-D HBPS-A2D525-502
Controller	PE Expert4
Oscilloscope	Teledyne Lecroy: Wavesurfer 3034z
Current sensor	Hioki: CT6862-05
Power meter	Hioki: PW6001

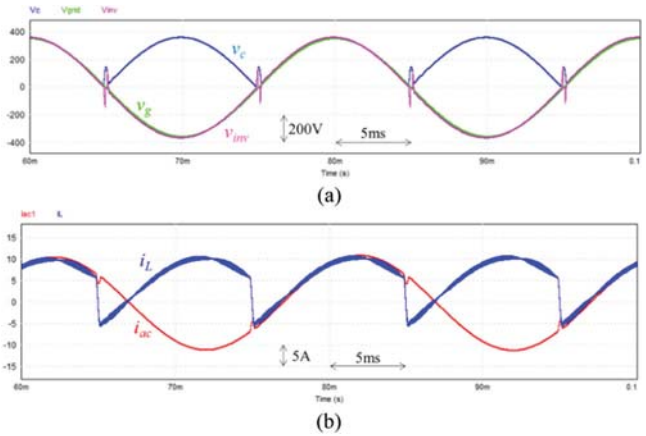


FIGURE 35. Simulation result in the steady-state: (a) Capacitor voltage v_c, grid voltage v_g, and inverter voltage v_{inv}; (b) dc inductor current i_L, and ac current i_{ac}.

in the simulations and experiments. Table 4 summarizes the equipment used in the experiments.

B. SIMULATION

Fig. 35 presents the steady-state simulation results for $P_{ref} = 1600$ W, $Q_{ref} = -1200$ var, PF = 0.8, and $V_g = 280$ V_{rms}. Fig. 36 shows the magnified waveforms near unfolding. During the unfolding sequence period (USP), two-cycle unfolding mode, three-cycle freewheeling mode, reverse-polarity PWM mode, and regular-polarity PWM mode are sequentially executed. At the end of the USP, the capacitor voltage and dc inductor current settle at the target values, and transients in the normal mode are not observed. Fig. 37 shows the ac current reference and ac current. Other than USP, the ac current follows the ac current reference well, and the THD is 3.35%.

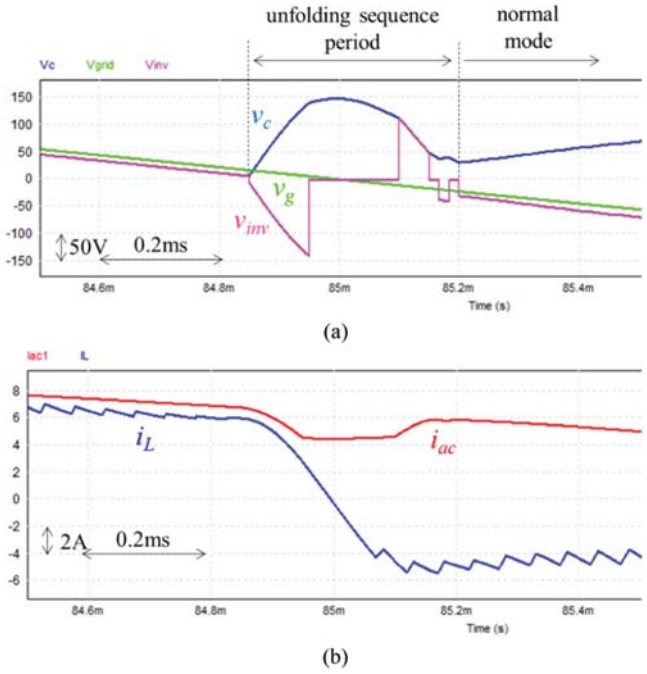


FIGURE 36. Simulation result: Zoomed-in waveforms near unfolding: (a) Capacitor voltage v_c, grid voltage v_g, and inverter voltage v_{inv}; (b) dc inductor current i_L and ac current i_{ac}.

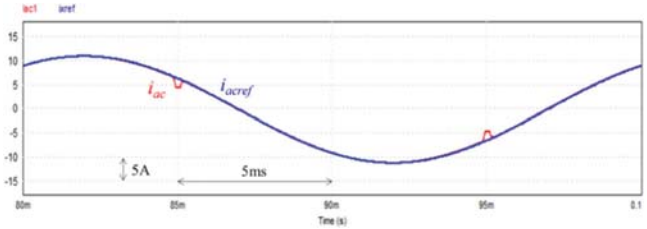


FIGURE 37. Simulation result: Ac current reference i_{acref} and ac current i_{ac}.

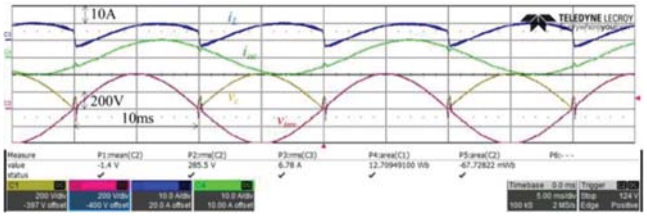


FIGURE 38. Experimental results: Steady-state waveforms.

This is much better than that shown in Fig. 7, where unfolding is simply conducted.

C. EXPERIMENTAL VERIFICATION

Fig. 38 shows the steady-state experimental waveform. The circuit conditions are the same as those shown in Fig. 35. Fig. 39 shows the magnified waveforms near unfolding. Similar to Fig. 36, the unfolding sequence is executed as intended.

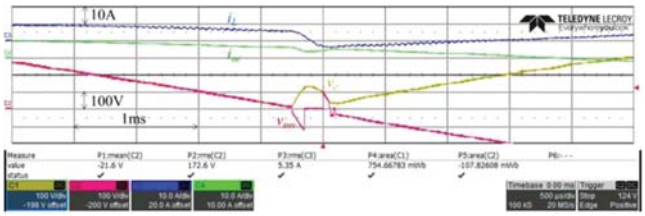


FIGURE 39. Experimental results: Waveforms near zero crossing.

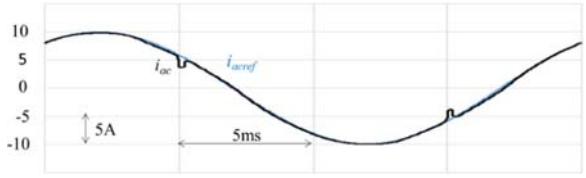


FIGURE 40. Experimental results: Zoomed-in ac current (in black) and ac current reference (in blue).

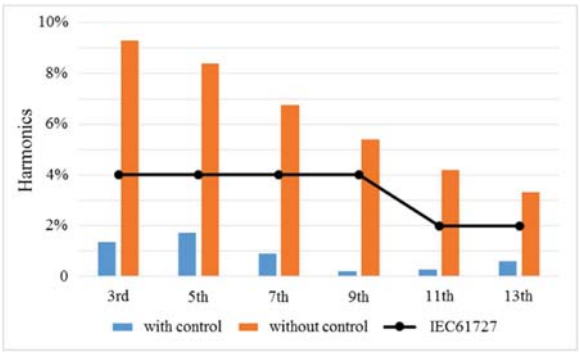


FIGURE 41. Harmonic contents of the ac current (PF = 0.9).

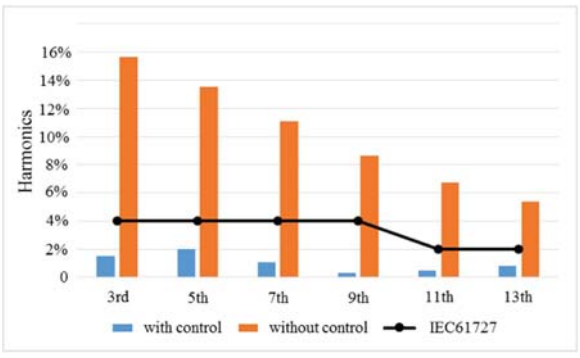


FIGURE 42. Harmonic contents of the ac current (PF = 0.8).

Fig. 40 shows the ac current, and the THD is 4.15%. No overshoot is observed in the ac current.

Table 5 lists the steady-state characteristics with various real and reactive powers with a total VA = 2000 VA, with the left and right halves of the table showcasing the powering and regenerating modes, respectively. The efficiency is measured using a very accurate virtual transformer-based

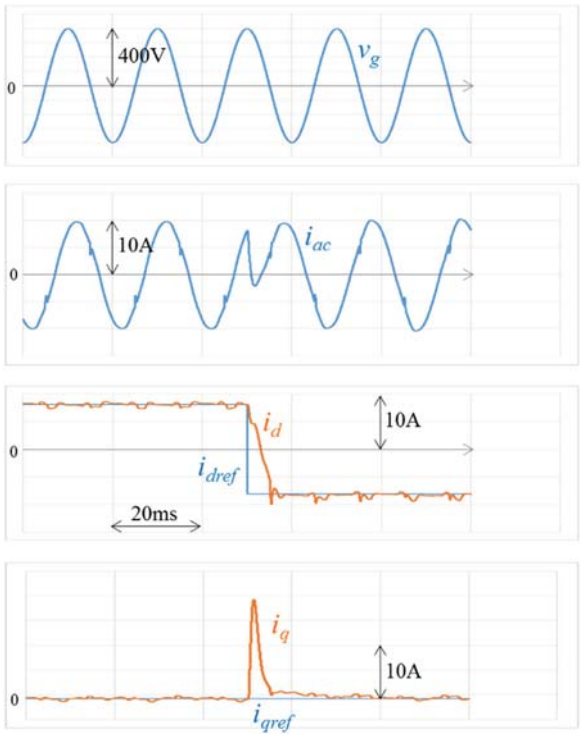


FIGURE 43. Experimental results: Transient response.

back-to-back asynchronous loss measurement method [29]. The measurement accuracy is approximately 0.006%. The efficiency decreases with decreasing PF, but still exceeds 99% even with PF = 0.5.

The harmonic contents of the ac current for the cases of PF = 0.9 and PF = 0.8 are described with upper limit values specified by IEC61727 in Figs. 41 and 42, respectively. The harmonic contents of the ac current without the new control scheme is shown in each figure. The fundamental component (100%) is abbreviated. The black line shows the upper limits by IEC61727. Harmonic contents with the control case are in blue, those without control are in orange. Therefore, the harmonic contents by the proposed scheme are well below the limit. The harmonics without the new control scheme are significantly worse than those with the proposed scheme.

Fig. 43 illustrates the transient responses from $P_{ref} = 1600$ W and $Q_{ref} = -1200$ var to $P_{ref} = -1600$ W and $Q_{ref} = -1200$ var. As discussed in Appendix A, d- and q-axis current control is achieved by estimating the virtual orthogonal component using a sinusoidal wave observer. The d- and q-axis currents are shown in Fig. 43. The d-axis current follows the d-axis current reference within 7 ms.

V. COMPARISON BETWEEN THE CONVENTIONAL AND PROPOSED SCHEMES

Table 6 shows comparison of non-unity power factor operation schemes. As already stated in the introduction section, Tian et al. [8] and Fonkwe [9] need additional circuit to handle reactive power. Han et al. [34] connects "dc link" circuit when

TABLE 5. Experiment Result: Steady-State Characteristics (Total VA = 2000 VA)

Powering:					Regenerating:					
P [W]	Q [VAR]	Power Factor	$V_{ac\ rms}$ [V]	$I_{ac\ THD}$ [%]	P [W]	Q [VAR]	Power Factor	$V_{ac\ rms}$ [V]	$I_{ac\text{-}THD}$ [%]	Average Efficiency* [%]
2001	63	1.000	280.1	2.33	–1995	81	–0.999	279.4	1.50	99.76
1913	–591	0.955	282.9	3.17	–1885	–661	–0.944	282.0	3.19	99.75
1816	–837	0.908	284.0	2.92	–1779	–904	–0.892	283.3	3.08	99.74
1617	–1174	0.809	285.5	4.15	–1579	–1220	–0.791	284.9	3.77	99.70
1441	–1376	0.723	286.4	4.80	–1391	–1431	–0.697	285.9	4.12	99.66
1003	–1699	0.508	287.8	5.40	–964	–1734	–0.486	287.4	5.77	99.50
40	–1981	0.020	288.9	6.25						

*The average efficiency is calculated using the measured efficiencies during the powering and regenerating operations based on [29]

TABLE 6. Comparison of Non-Unity Power Factor Operation of Unfolding Inverters

literature	dc/dc converter	scheme for non-unity pf operation		pf range	THD	efficiency
		additional circuit	control scheme			
Tian [8]	high frequency link converter	needed	none	0 to 1, lead/lag	N/A	N/A
Fonkwe [9]	flyback module integrated converter with pseudo dc link	needed (current decoupling circuit)	none	0 to 1, lead/lag	4% with pf=0	N/A
Li [10]	buck converter + inductor	none	quasi-sinusoidal current reference	0.86 to 1, lead/lag	26% with pf 0.9	N/A
Han [34]	Cuk converter	"dc-link" circuit is added	whole PWM operation when dc-link is connected	0 to 1, lead/lag with PWM inverter	3.04% with pf 1.0, 3.55% with pf 0.5	N/A
Min [35]	boost/buck converter with coupled inductors	none	partial PWM (a few milliseconds) operation before and after zero crossing	N/A	N/A	96.5% with pf 1.0
Han [36]	bridgeless Cuk-derived inverter		partial PWM (a few milliseconds) operation before or after zero crossing	>0.85, lead/lag	3.27% with pf 0.85 lag, 3.53% with pf 0.85 lead	96.6%
Renaudineau [37]	dual buck	none	partial PWM (a few milliseconds) operation before and after zero crossing,	0 to 1, lead/lag	harmonic complies with IEEE519	max 96.8%
proposed scheme	multi-level buck converter [6], [7]	none	control (a few-cycle PWM)	0 to 1 lead [39], 0 to 1 lag (this paper)	<5% with 0 to 1 pf lead, <5% with 0.7 to 1 pf lag	>99%

the inverter needs to output reactive power, and the inverter operates as the conventional PWM inverter. Li et al. [10] uses quasi-sinusoidal current reference, and it results in very large distortion. Min et al. [35], Han [36], and Renaudineau et al. [37] use partial PWM operation (a few milliseconds) before or after voltage zero crossing, thus it increases switching loss. Combining the leading pf operation previously reported in [39] and the lagging pf operation proposed in this paper, our scheme achieves 0 to 1 leading/lagging pf operation without additional circuit.

A comparison of the PF–THD relation is shown in Fig. 44. Li [10] applied a quasi-sinusoidal waveform (QSW) current

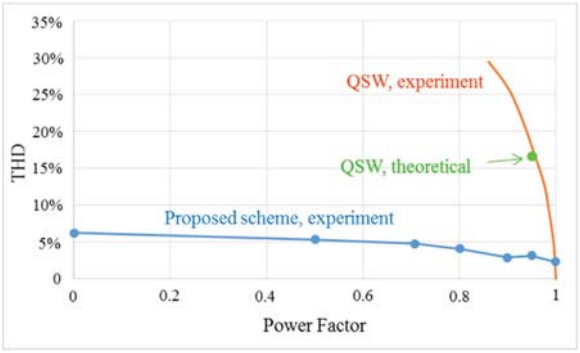


FIGURE 44. Comparison of THD.

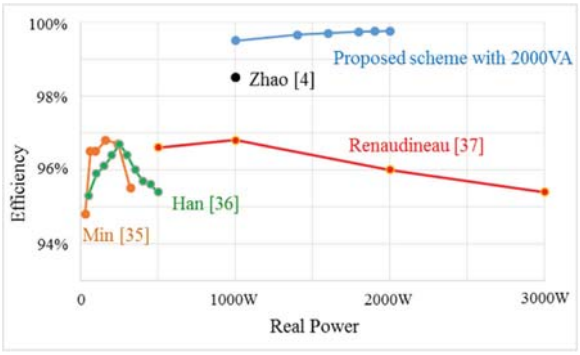


FIGURE 45. Comparison of efficiency.

reference to handle the reactive power. The orange curve represents the theoretical THD obtained using the QSW scheme. The green dot presents the experimental data obtained using the QSW method with a PF = 0.95 and THD = 16.7%. The blue curve shows a plot of the THD data in the powering mode of the proposed method in Table 5. For the QSW scheme, the THD exceeds 5% with a PF > 0.995. Additionally, the range of PF operation is limited to >0.86. By contrast, the THD of the proposed method is <5% within the range of PF operation of 0.7–1.

Furthermore, research presenting efficiency data is scarce. Fig. 45 depicts a comparison of the efficiency data. The orange curve shows the data reported by Min et al. [35], which requires no additional circuit. The green curve shows the data reported by Han et al. [36], and the red curve shows that by Renaudineau et al. [37]. The black dot shows one point measurement by Zhao et al. [4]. The data in [4], [35], [36], and [37] are measured at a unity PF. The data in [37] contain measurements for more than 3000 W, but these efficiency values are lower and are omitted in this graph. The blue curve shows the data of the proposed scheme plotted using Table 5, with total VA = 2000 VA, indicating variable PF. For instance, at 1617 W on the horizontal axis (real power), the PF = 0.809, which can be verified from Table 5. The inverter ratings in [4], [35], [36], and [37] were 320, 500, 5600, and 1000 W, respectively. Hence, comparing the efficiency of inverters with different ratings in the same condition is difficult. Nonetheless, the efficiency of the proposed inverter is significantly higher than those reported in previous studies.

VI. CONCLUSION

Theoretical analysis and simulations are performed to clarify that the proposed novel control scheme can be used to operate grid-connected unfolding inverters with a lagging PF. Furthermore, experiments are conducted to verify the simulation results. When the unfolding inverter is operated with a lagging PF, and the inverter is unfolded at voltage zero crossing, dc voltage quickly increases. Using this phenomenon, the dc inductor current is reduced to the opposite polarity during the freewheeling mode, and the dc voltage is reduced in reverse-/regular-polarity PWM mode. Moreover, target values for a smooth return to the normal mode are calculated using a virtual PWM inverter. In addition, the unfolding timing is slightly shifted forward to reduce the ac current overshoot. Compared with conventional methods, our proposed scheme deals with reactive power using only control, and no additional circuit is required; however, only a few PWM cycles are required. The THD of our scheme is much smaller than that of conventional methods. Based on the reactive power operation range described in Fig. 1, grid-tie inverters are deemed essential to operate from a lagging 0.9 PF to a leading 0.9 PF. Within this range, the THD of the inverter is within 5%. If the THD constraint is to be neglected, the PF operation range of our inverter covers the entire range from PF = -1 to PF = + 1, as shown in Table 5. Thus, an unfolding inverter can be operated for both leading [39] and lagging PF. In addition, both powering and regenerating are possible; thus, it is verified that an unfolding inverter can be operated in four-quadrant operation. The harmonics are compliant with grid code IEC61727. The efficiencies are 99.76% with PF = 1.0 and 99.50% with PF = 0.5, which are very high.

APPENDIX A
CURRENT CONTROL OF A GRID-CONNECTED INVERTER

When an HEECS is applied to a grid-connected inverter, the inverter output voltage is synchronized with the grid voltage, and the real and reactive output powers are controlled to match the command values, as shown in the control block diagram in Fig. 46. The current reference generator calculates the current references i_{dref} and i_{qref} from the real power reference P_{ref}, the reactive power reference Q_{ref}, and the grid electrical angle θ_g detected by the phase-locked loop (PLL). The ac current i_{ac} is input into a sinusoidal wave observer [39], and the orthogonal components are estimated and converted into i_d and i_q. These are compared with the current references i_{dref} and i_{qref}, and the errors serve as inputs for the current controllers. The output signal, v^*_{inv}, of the x-axis controller becomes the inverter voltage command. The sign of v^*_{inv} is used to select the switching pattern of the unfolding inverter. The absolute value of v^*_{inv} becomes the voltage reference to the voltage controller of the dc/dc converter.

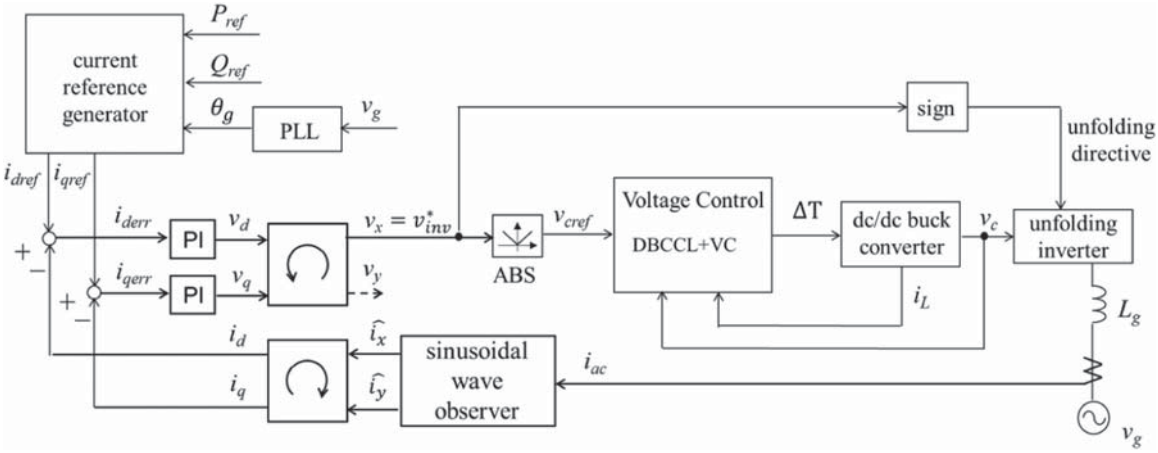


FIGURE 46. Control block diagram of current control for the grid-connected inverter based on HEECS.

The voltage control block shown in Fig. 46 generates a fully rectified sinusoidal voltage that is synchronized with the grid voltage. This block is realized by DBCCL + VC (Fig. 7).

APPENDIX B
EQUATION OF ΔU AND ΔT FOR SMOOTH LANDING TO THE NORMAL MODE

In general, a time delay exists between the detection and the control pulse output, and a one-step state prediction is required. In other words, the controller detects state values at t = kT, predicts state values at t = (k + 1)T, calculates the desired output pulse width to be output in the time section [(k + 1)T, (k + 2)T], sets the pulse width on the hardware register at t = (k + 1)T, and aims for the control variable at t = (k + 2)T to match the target value.

The state values at t = (k + 2)T can be predicted as follows:

$$\begin{bmatrix} \widehat{v_c}(k+2) \\ \widehat{i_L}(k+2) \end{bmatrix} = F \begin{bmatrix} \widehat{v_c}(k+1) \\ \widehat{i_L}(k+1) \end{bmatrix} + G_1 \Delta T + G_0 \widehat{i_{dc}}(k+1) \tag{A-1}$$

The dc current when the reverse/regular-polarity PWM mode is used is calculated using

$$\widehat{i_{dc}}(k+1) = \Delta U/T \cdot \left|\widehat{i_{ac}}(k+1)\right| \tag{A-2}$$

Substituting this into (A-1),

$$\hat{x}(k+2) = F\hat{x}(k+1) + \begin{bmatrix} g_{11} & g_{01}\left|\widehat{i_{ac}}(k+1)\right|/T \\ g_{12} & g_{02}\left|\widehat{i_{ac}}(k+1)\right|/T \end{bmatrix} \begin{bmatrix} \Delta T \\ \Delta U \end{bmatrix}$$

$$= \mathrm{F}\hat{x}(k+1) + \tilde{G}\begin{bmatrix} \Delta T \\ \Delta U \end{bmatrix} \tag{A-3}$$

Replacing the predicted values at t = (k + 2)T with the target values x_{ref}(k + 2) and solving equation for ΔT and ΔU, we obtain

$$\begin{bmatrix} \Delta T \\ \Delta U \end{bmatrix} = \tilde{G}^{-1}\left(x_{ref}(k+2) - F\hat{x}(k+1)\right) \tag{A-4}$$

Here, a positive ΔU is interpreted as reverse polarity, and a negative ΔU is interpreted as regular polarity.

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PE－24－068
PSE－24－080
SPC－24－122

高効率 HEECS インバータの損失低減に関する新しい展開

河村篤男＊　Van-Long Pham、味口泰彦、小原秀嶺（横浜国立大学）

New Direction on Loss reduction of high efficiency HEECS inverter

Atsuo Kawamura, Van-Long Pham, Yasuhiko Miguch, Hidemine Obara
(Yokohama National University)

In order to reduce the losses of the HEECS inverter, we consider two methods, focusing on the inductors and the capacitors losses. First, the inductance is changed and the inverter losses are measured using the VTASLM method. Second, the capacitors are replaced and the losses are measured.

キーワード：インバータ，高効率，測定法，HEECS
(Keywords: Inverter, High efficiency, Measurement, HEECS)

1.　はじめに

著者らは、図１に示した HEECS インバータによる電力変換効率 99.9%を目指した DC-AC 電力変換の実現を理学的な見地から検討してきた[1]。WBG(wide-band-gap)デバイスを用いたインバータの高効率実測が複数報告[1-8]されているので、その測定精度が明記されたものに関してはそれを含めて、出力と効率の最新報告例を図２に示した。これによると 99.5%以上の効率が最新の高効率インバータの動向と言える。

著者らのグループでは、測定精度の高い測定法（VTASLM 測定法）を提案して、測定器の較正および測定データの統計的な処理により損失の測定精度が 0.006%程度まで高められることを示した[7]。その測定手法に基づいて、文献（9,10）では、損失を体系的に最小化する手法が提案された。しかし、損失最小化のすべての手法が検討されてはいなかった。そこで、本論文では未検討の方向からの損失低減のアプローチをしたので、報告する。

２章では、これまでの損失低減の経緯を概説する。3.1 章では、インダクタンスの最適化に関して検討を行い、3.2 章では、キャパシタンスの最適化に関しての検討を報告する。3.3 章の考察では、さらなる損失低減の方向に関して考察を行う。4 章は結論である。

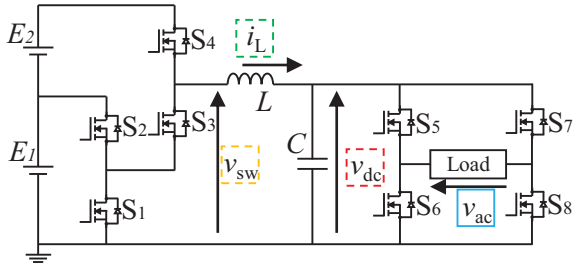

図１　２電源 HEECS インバータの回路トポロジー
Fig. 1. Two battery HEECS inverter.

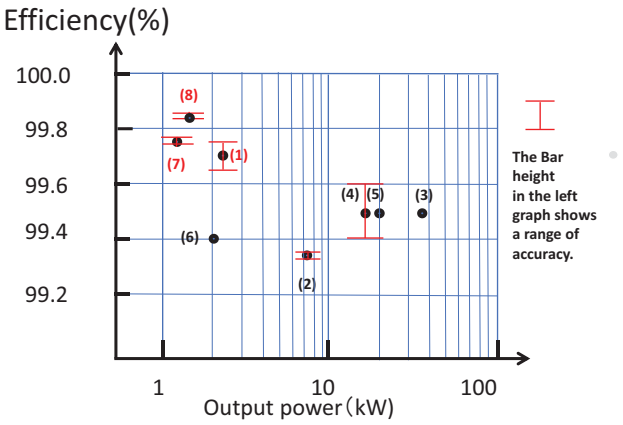

図２　高効率インバータの報告例(文献番号参照)
Fig.2. Survey of high efficiency literatures on inverter operation

2.　損失最小化の手法[9,10]の復習とこれまでの経緯

2.1 損失最小化法の復習

文献(9,10)で提案した損失最小化手法では、優先順位を考慮して、自由度を以下に示す項目１から４に分類した。重要度は、１が高く、２，３，４と優先度は下がると考えた。従って、項目４から項目３にかけて、順番にパラメータの最適化を行い、電力変換効率の最大化を実現してきた。

【項目１】: 前提条件として、表１に示す基本仕様を設定する。（デバイスの電圧余裕、スイッチング周波数、出力電圧の歪率）

【項目２】: 前提条件としての回路トポロジーを選び、今回は、図１の HEECS インバータとした。他の回路候補は、文献（9）に詳しい。

【項目３】: 準仕様としてのスイッチングデバイス（チョッパ部と折り返しインバータ）とチョッパ部のフィルタの回

表１　損失最小化被試験インバータの基本仕様
Table 1 Conditions for inverter under test

デバイスの電圧余裕	出力電圧の 50%
スイッチング周波数	16 kHz
出力電圧ひずみ率	1%程度

表２　準仕様パラメータ
Table 2 Quasi-free Parameters

チョッパデバイス	Ron=17mΩ(typ) SCT3017AL(Rohm)
折り返しインバータデバイス	Ron=3.7mΩ CAS325M12HM2 (Wolfspeed)
インダクタ L	1.25mH(18mΩ) (フェライト) (IPEC)
キャパシタ C	8μF (3.5mΩ) (フィルム) (ARCOTRONICS)
制御	DB（Deadbeat） 力行及び回生運転 文献(11)
PCB	175μ 銅厚 （数 mΩ）(1) （P 板）

表３【項目４】の自由パラメータの最適化
Table 3 Free parameters on item 4

E_1とE_2の比率
ドライバ回路定数
可変デッドタイム制御
有効及び無効電力の選定
チョッパ部の電流センサレス制御

路パラメータを考えた。さらに、PCB の導体厚みの条件と制御方式（力行と回生運転）もこれに含めた。これらを表２に示す。スイッチングデバイスは、選定時に市場で得られる最上の条件に合うものとした。

【項目４】: 仕様としての自由パラメータは、上記 3. 以外のパラメータであり、具体的には、以下の 5 点となる。: (a) E_1 と E_2 の比率、(b) ゲートドライバ回路の定数、(c) 可変デッドタイム制御とその定数、(d) インバータと系統と連系（力行および回生）する電流の有効および無効電力の比率、(e) チョッパ部の電流センサレス制御。これらを表３にまとめた。

2.2　これまでの経緯

文献(9)では、【項目４】のすべての項目に関して、損失の精密測定法（VTASLM）の提案である文献(7)の測定法に従って最適化した。さらに、文献(8)では、文献(9)よりも踏み込んで、項目３の最適化は一部のみ検討が行われた。その結果は、図２に反映している。

次章では、チョッパ部の回路パラメータであるインダクタンスとキャパシタンスに関して項目３レベルでの検討を行う。

3.　自由パラメータであるインダクタンスとキャパシタンスの最適化

3.1　インダクタの損失の最少化

インダクタの損失は銅損、基本波鉄損、高調波電流損の三つの損失要素から構成されると考えられる(1,12)。文献(1)では、その３者の大きさは、ほぼ等しいことが実測されている。これらのうち、銅損を減らすには、巻き線抵抗を低減することが重要である。銅線を太くすると、インダクタの体格が大きくなり、基本波鉄損が増加すると考えられる。さらに、高周波電流損を減らすには、高調波電流を減らすことが重要であるが、そのために、インダクタンスを増やす対策が考えられる。これら３つの要素は、お互いに関連していて、最大効率を求める場合は、通常の電力密度を最大化するようなインダクタの設計とは異なるアプローチが必要となる。

そこで、文献(8)では、文献(9)のインダクタ（表２のインダクタであり、これを＃１インダクタ(#1L)と呼ぶ。）を改良して、巻き線抵抗の小さいもの製作し（これを＃２インダクタ(#2L)と呼ぶ）、損失を実測した。しかし、体格が大きくなって、基本波鉄損の損失が増大したと考えられ、損失の低減幅はわずかであった。そこで、本論文では、体格も考慮した新しいインダクタ（＃３インダクタ(#3L)と呼ぶ）を試作した(13)。これらの基本特性をまとめたものを表４に示す。特に、磁路の体積比が重要な指標であり、＃３インダクタでは、巻き線抵抗は＃２に比べ大きくなったが、磁路体積を＃２よりも小さく設計した。

表４　３種類の試作インダクタンス
Table 4 3 kinds of inductors

番号	L(mH)	R(mΩ)	材質	磁路体積比
#1	1.27	15.06	フェライト	1.00
#2	2.06	5.24	フェライト	3.91
#3	1.25	11.66	フェライト	1.51

これら３種類のインダクタの特性を実測した結果を表５にまとめて示してある。

まず、50Hz の正弦波電流をインダクタに流して、電流をパラメータに取り、直接法により、全損失を求めた。ただ、この測定精度は非常に悪い(1)。さらに、基本波鉄損を、この基本波導通の全損失から導通損（LCR メータで測定した抵

抗から計算したジュール損）を差し引いて求めた。なお、電流値は、HEECS インバータ運転において、1200W から 1700W の出力に対応する電流値を選んだが、このうち 3 通りのデータを表 5 に載せた。

表 5　3 種類のインダクタの特性実測表
Table 5 characteristics of 3 kinds of inductors

	電流(A)	4.3	4.64	4.97
	等価出力(W)	1300	1400	1500
#1L	基本波鉄損(W)	-0.011	-0.019	-0.017
	基本波銅損(W)	0.3143	0.3660	0.4199
	高調波損(W)	0.0717	0.0583	0.0417
	測定合計(W)	0.375	0.405	0.445
	実測効率(%)	99.827	99.826	99.825
#2L	基本波鉄損(W)	0.1652	0.2113	0.2333
	基本波銅損(W)	0.1048	0.1221	0.1401
	高調波損(W)	0.1550	0.1317	0.1217
	測定合計(W)	0.425	0.465	0.495
	実測効率(%)	99.827	99.827	99.828
#3L	基本波鉄損(W)	0.0055	0.0162	0.0144
	基本波銅損(W)	0.1545	0.18377	0.21599
	高調波損(W)	0.0492	0.02	0.00023
	測定合計(W)	0.2092	0.2200	0.2306
	実測効率(%)	99.836	99.836	99.835

次に、インダクタを HEECS インバータに組み込んで、力行と回生の運転時のインダクタの平均全損失を直接法で測定した。その実測値から、50Hz で測定した導通損と基本波鉄損を差し引いたものを高調波損として仮定して、この表に記入した。この高調波損には、高調波電流による渦電流損と、高調波電流による鉄損（ヒステリシス損）が含まれる。また、その時の VTASLM 測定法に基づく全電力変換効率も記入した。この測定精度は非常に高い(7)。

この表から観測されることは、以下となる。

（1）＃２インダクタ(#2L)は、銅損は小さいが、基本波鉄損および高周波損が、他の 2 種類のインダクタと比較して大きい。

（2）＃３のインダクタ(#3L)は、銅損は＃１と＃２のインダクタの中間に位置するが、鉄損と高周波損は、ほぼ＃１のインダクタと同程度である。

＃３のインダクタは＃１のインダクタに比べて磁路の体積が 1.5 倍程度であるのに対して、＃２の場合は、約 3 倍となっている。しかし、表 5 の損失の大きさの関係はこのような定性的な予想値とは一致しない。インダクタの総損失の測定法は、両端の電圧と電流の積から損失を求める直接法であり、その精度が低いためと思われる(1)。

そこで、＃３のインダクタに関して、鉄損と高周波損に関して追加の測定を行ったので、その測定データを図 3 と図 4 に示す。図 3 は 50Hz の電流をパワーアンプから流して測定したもので、高調波電流は含まれていない。また、材質が

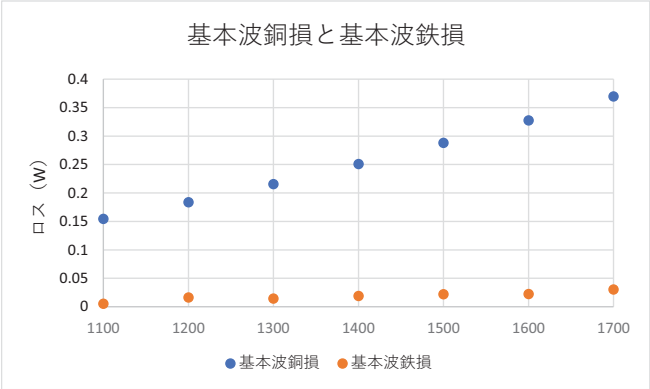

図 3　#3L の基本波銅損と基本波鉄損
Fig. 3. Joule and iron loss of #3L at the fundamental frequency

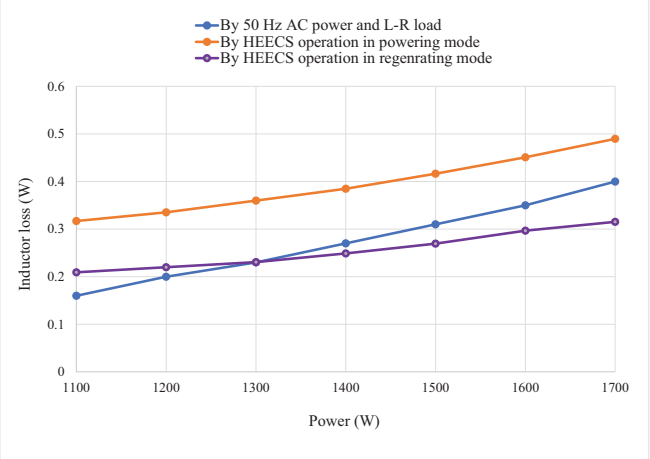

図 4　#3L の損失の比較
（基本波のみ、力行および回生運転）
Fig. 4.　Loss of #3L at the fundamental frequency, powering and regeneration operation

フェライトであり、電流の動作点は、定格電流（設計点）の 20%程度であるので、鉄損は非常に小さい。図 4 は、HEECS インバータに組み込んだ時のデータであるので、高調波電流を含んでおり、また、回生運転時には、電流の向きは逆になっている。この図から観察されることは、力行時には 50Hz 駆動時とほぼ同様な特性を示しているが、回生時には、回生電力が小さい領域では、高調波損が大きくなっている点である。その原因としては、この電力領域では高調波電流が大きくなっている可能性、および電流センサの正方向と負方向の測定値にずれがある可能性などの理由が考えられる。

最後に、損失の精密測定法である VTASLM 法(7)に基づいて、＃３のインダクタンスを用いた HEECS インバータの効率を測定した。その効率と測定精度を図 5 と図 6 に示す。出力が 1300Wの時に、変換効率 99.836±0.004%が実測された。この実測値は、＃２のインダクタの時の効率よりもわ

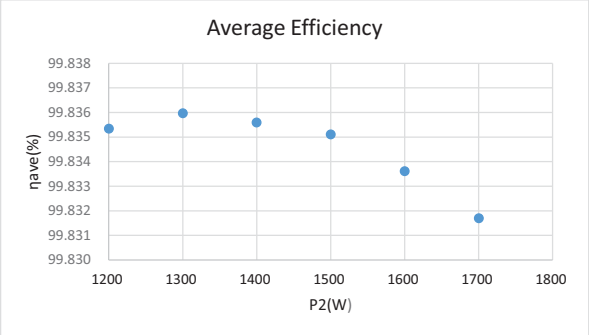

図５　SiC-HEECS インバータの効率
(#3L)
Fig.5 Measured efficiency of SiC HEECS Inverter with #3L

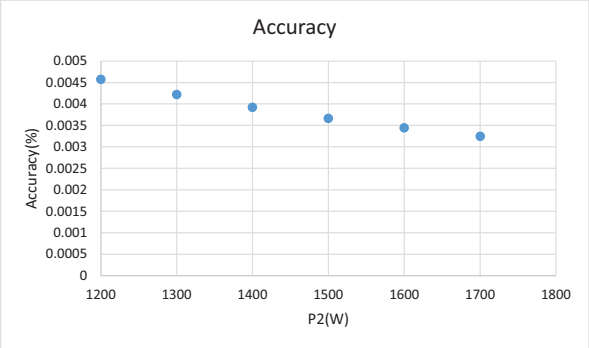

図６　SiC-HEECS インバータの効率測定精度(#3L)
Fig.6 Accuracy of SiC-HEECS Inverter efficiency measurement with #3L

ずかに向上している。測定精度を勘案しても、＃２のインダクタよりも＃３のインダクタを用いる方が高い効率が得られたと考えられる。

3.2　C の最適化

次に、チョッパ部のフィルタのキャパシタの大きさに関して検討を行った。

HEECS チョッパ部のキャパシタの材質は、フィルムなので、キャパシタでの損失は非常に小さいと考えられる。むしろ、インダクタの波形は、図７のような波形となるので（文献１）、折り返しインバータでの電圧と比較すると、進み電流を折り返したような形（半波整流の電流波形）と考えられる。従って、キャパシタの静電容量が大きいと、半波整流の電流の実効値が大きくなる。その結果、インダクタやスイッチングデバイスでの導通損が増加する傾向となると考えられる。

これを式で表現すると以下となる。50Hz でのフェイザーを考え、力率１の負荷電流の振幅を I_{load}、キャパシタの電流を I_c と定義すると、負荷電流が力率１であれば、キャパシタ電流とは位相が 90 度ずれているので、インダクタの電流の振幅 I_L は、次式で近似できる。

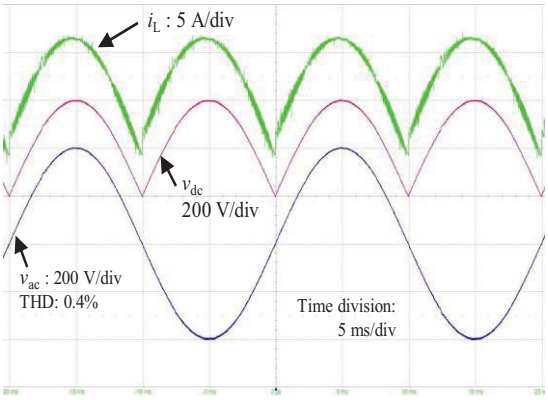

図７　HEECS インバータの各部の波形(1)
Fig. 7 Three kinds of waveforms at 2.2 kW output of HEECS Inverter in Fig. 1(1)

$$I_L=SQRT(I_{load}^2+I_c^2) \quad \text{----} \quad (1)$$

$$I_c=abs(j\omega CVac) \quad \text{----} \quad (2)$$

ただし、キャパシタの静電容量を C、折り返しインバータの出力電圧の振幅を Vac と定義する。
さらに、疑似力率 pf_{pseudo} を次式で定義する。

$$Pf_{pseudo}=abs(I_c/I_L) \quad \text{------} \quad (3)$$

例えば、8uF のフィルムキャパシタンス（R_{ESR}=3.5mΩ）を選んだ場合、出力電力が 1300W（at 302Vrms）の条件では、I_{load}=4.3 (A)、I_c=0.76(A)となるので、pf_{psuedo}=0.98 となる。

各部での導通損は、I_L の 2 乗に比例するので、C は小さいほど導通損は減少するが、電圧制御としてデッドビート制御を行っているので、C が小さいと不安定になる傾向があるので、電流の高調波成分が増加する。

文献(7-9)では、C は８μF で固定してきたが、これを 8.0μF,7.5μF,7.0μF, 6 .5μF と変化させて損失を VTASLM 法(7)で測定したものを図８に示す。なお、この実験の過程で、操作ミスによりスイッチングデバイス(図１の S3 と S4)を破損したので、この４点の C 変化による効率の測定データはスイッチングデバイスが、3.1 節の測定データとは、値が少し異なっている。従って、図８を new PCB#5 での測定データと呼ぶことにする。

この図から、C 変化による効率向上は、7uF 付近でわずかに認められるが、それは測定誤差の範囲内と言える。なお、3. 1 節の図５では、8μF の C で、効率 99.836%(at 1300W 出力)を実測しているが、この図５と図８では使用したパワーデバイスは異なっている。

3.3　考察

２章で概説した、文献（9,10）で提案された損失最適化のアプローチに関しては、本論文ですべての【項目３】と【項目４】の組み合わせをほぼ終了した。残りの損失向

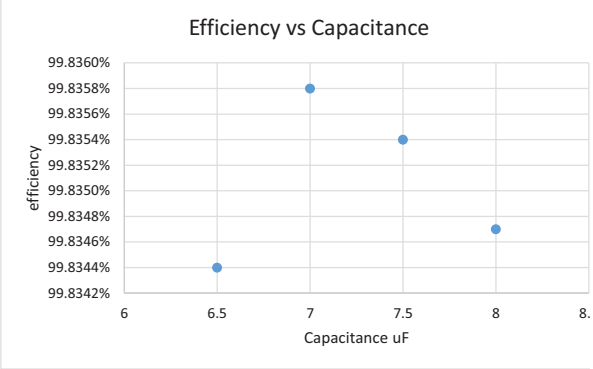

図 8　キャパシタンス変化時の最大効率 (newPCB#5)
Fig. 8 Maximum efficiency when the capacitance is changed(new PCB#5)

上の可能性は、パワーデバイスの改良によるスイッチング損と導通損の低減と考えられる。

4. まとめ

測定精度の高い電力変換器の損失測定法（VTASLM 測定法(7)）を採用して、２電源 HEECS インバータの損失低減手法(9,10)が提案されたので、この２つの手段によって、損失の最小化を追求した。すでに様々な最適化が検討されたので[8,9]、実証が未検討で残っている部分を検討した。

特に、本論文では、インダクタとキャパシタのパラメータを最適化することを実験的に検討した。

インダクタに関しては、巻き線抵抗、基本波鉄損、高調波損失の３つが連動していることに注目し、新しいインダクタを試作して、実測した。また、キャパシタに関しては、導通損と制御性能が損失に関連していることに注目して、各種キャパシタンスの値で損失を実測した。その結果、現状での最高効率としては、電力変換効率 99.836±0.004％（1300W 出力）が実測できた。

今後の損失最小化のためには、パワーデバイスの性能向上の進展によるところが大きいと考えられる。

なお、HEECS インバータの系統連系への応用に関しては、文献（14,15）に詳しく、遅れや進みの力率負荷でも制御を工夫すれば安定に動作することが報告されている。

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